

MC722

Organização de Computadores Teoria e Prática

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Arquitetura de Computadores

Micro-Arquitetura

"COD" - (Capítulo 4)

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Micro-Arquitetura

- Micro-Arquitetura
 - Introdução
 - Recursos
 - MIPS Mono-Ciclo
 - » Lw
 - » Sw
 - » R-Type
 - » Beq
 - » j
 - MIPS Multi-Ciclos
 - » Lw
 - » Sw
 - » R-Type
 - » Beq
 - » j

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Introdução

- Micro-arquitetura: como está implementada a arquitetura em hardware
- Processador:
 - Datapath: blocos funcionais
 - Controle: sinais de controle

Application Software	programs
Operating Systems	device drivers
Architecture	instructions registers
Micro-architecture	datapaths controllers
Logic	adders memories
Digital Circuits	AND gates NOT gates
Analog Circuits	amplifiers filters
Devices	transistors diodes
Physics	electrons

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Micro-Arquitetura

- Múltiplas implementações para uma mesma arquitetura:
 - Single-cycle
 - » Cada instrução é executada em um único ciclo
 - Multicycle
 - » A execução de cada instrução é dividida em uma série de passos menores
 - Pipelined
 - » A execução de cada instrução é dividida em uma série de passos menores
 - » Múltiplas instruções (parte de) executando ao mesmo tempo.

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Micro-Arquitetura

- Program execution time
$$\text{Execution Time} = (\# \text{ instructions})(\text{cycles/instruction})(\text{seconds/cycle})$$
- Definições:
 - Cycles/instruction = CPI
 - Seconds/cycle = clock period
 - $1/\text{CPI} = \text{Instructions/cycle} = \text{IPC}$
- Desafios na implementação de uma micro-arquitetura
 - Custo
 - Power
 - Desempenho

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Micro-Arquitetura

- **Processador MIPS (Microprocessor without Interlocked Pipeline Stages)**

- Vamos implementar um sub conjunto das instruções MIPS:
- R-type instructions: and, or, add, sub, slt
- Memory instructions: lw, sw
- Branch instructions: beq

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Micro-Arquitetura

- Estado da Arquitetura

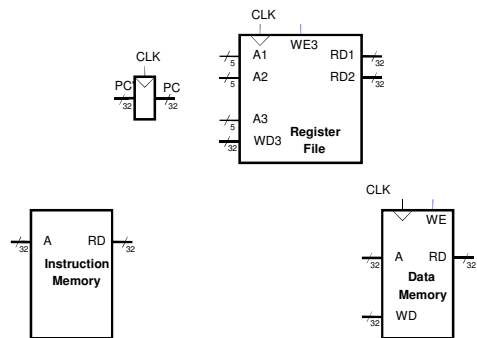
- Determina o estado do Processador em um dado instante de tempo

PC
32 registradores
Memória

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Micro-Arquitetura

- Elementos de estados do MIPS:



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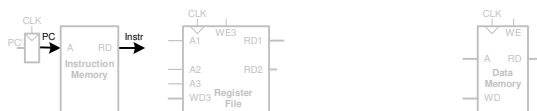
Processador MIPS Single-Cycle

- Datapath
- Controle

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Processador MIPS Single-Cycle

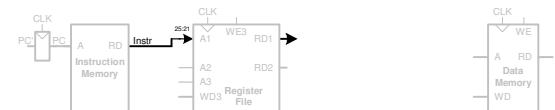
- Execução de lw
- 1: Fetch da Instrução



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Processador MIPS Single-Cycle

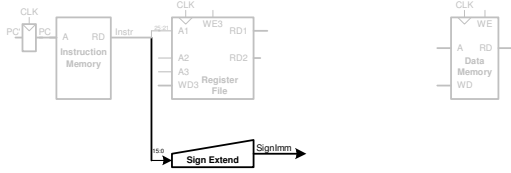
- Execução de lw
- 2: Lê o operando fonte do RF



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Processador MIPS Single-Cycle

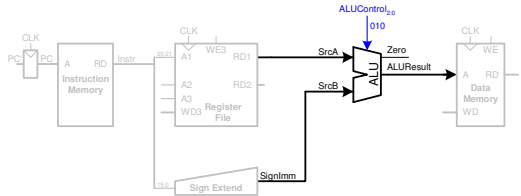
- Execução de lw
- 3: Sign-extend o imediato



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Processador MIPS Single-Cycle

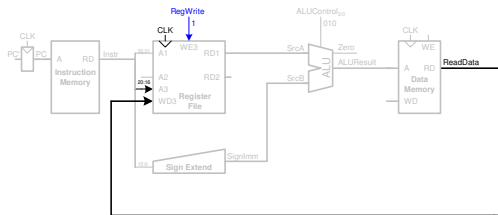
- Execução de lw
- 4: Calcula o endereço efetivo de memória



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Processador MIPS Single-Cycle

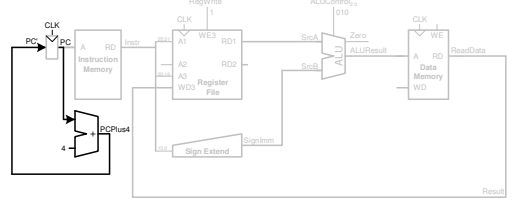
- Execução de lw
- 5: Lê o dado da memória e o escreva no RF



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Processador MIPS Single-Cycle

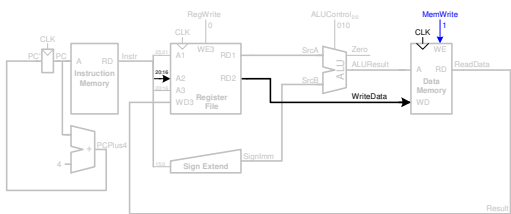
- Execução de lw
- 6: Determina o endereço da próxima instrução



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Processador MIPS Single-Cycle

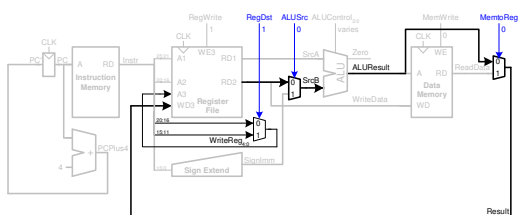
- Execução de sw
- Precisa escrever o valor do registrador na memória



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Processador MIPS Single-Cycle

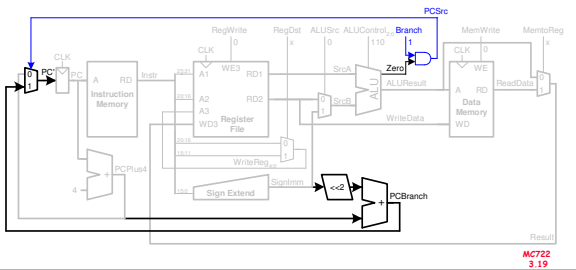
- Instruções R-Type: add, sub, and, or, ...
- Escrever ALUResult no RF
- Escreve em rd e não em rt



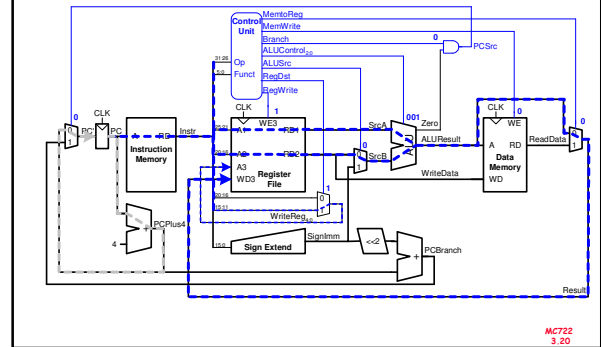
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Processador MIPS Single-Cycle

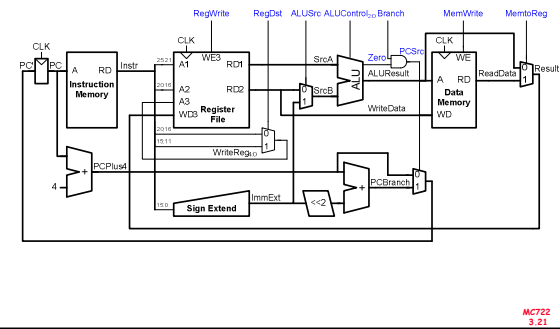
- Instrução beq
- Determina se os conteúdos dos registradores são iguais
- Calcula o endereço alvo do desvio (sign-extended immediate + PC+4)



Processador MIPS Single-Cycle - or

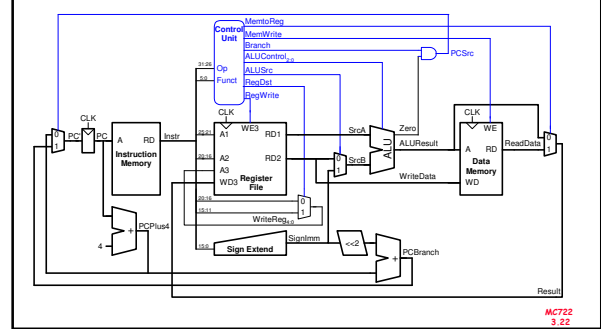


Processador MIPS Single-Cycle - sw



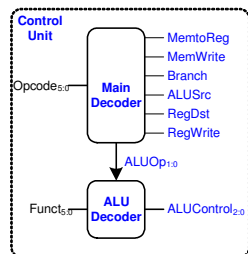
Processador MIPS Single-Cycle

- Unidade de Controle



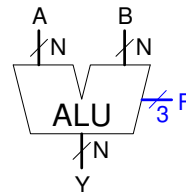
Processador MIPS Single-Cycle

Control Unit



Processador MIPS Single-Cycle

- ALU

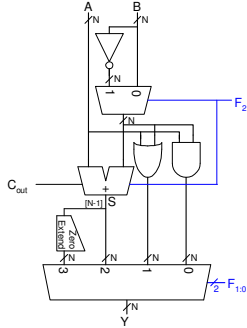


F _{2:0}	Function
000	A & B
001	A B
010	A + B
011	not used
100	A & ~B
101	A ~B
110	A - B
111	SLT

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Processador MIPS Single-Cycle

• ALU



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Processador MIPS Single-Cycle

• ALU Decoder

ALUOp _{1:0}	Meaning
00	Add
01	Subtract
10	Look at Funct
11	Not Used

ALUOp _{1:0}	Funct	ALUControl _{2:0}
00	X	010 (Add)
X1	X	110 (Subtract)
1X	100000 (add)	010 (Add)
1X	100010 (sub)	110 (Subtract)
1X	100100 (and)	000 (And)
1X	100101 (or)	001 (Or)
1X	101010 (slt)	111 (SLT)

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Processador MIPS Single-Cycle

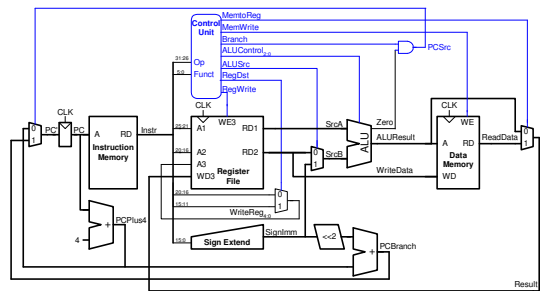
• Decodificador Principal

Instruction	Op _{5:0}	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	ALUOp _{1:0}
R-type	000000	1	1	0	0	0	0	10
lw	100011	1	0	1	0	0	0	00
sw	101011	0	X	1	0	1	X	00
beq	000100	0	X	0	1	0	X	01

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Processador MIPS Single-Cycle

• Extendendo a Funcionalidade: addi



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Processador MIPS Single-Cycle

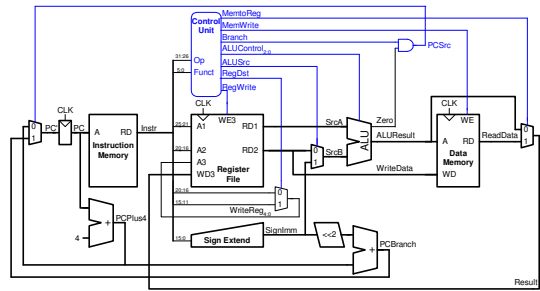
• Decodificador Principal

Instruction	Op _{5:0}	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	ALUOp _{1:0}
R-type	000000	1	1	0	0	0	0	10
lw	100011	1	0	1	0	0	1	00
sw	101011	0	X	1	0	1	X	00
beq	000100	0	X	0	1	0	X	01
addi	001000	1	0	1	0	0	0	00

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Processador MIPS Single-Cycle

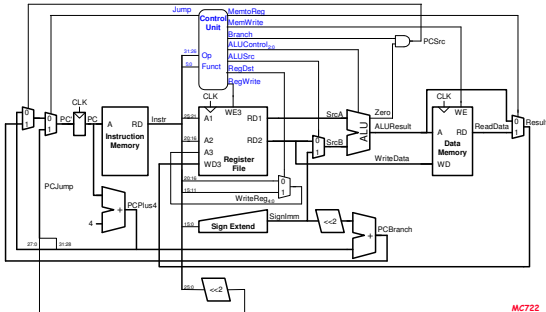
• Extendendo a Funcionalidade: j



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Processador MIPS Single-Cycle

- **Extendendo a Funcionalidade: j**



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Processador MIPS Single-Cycle

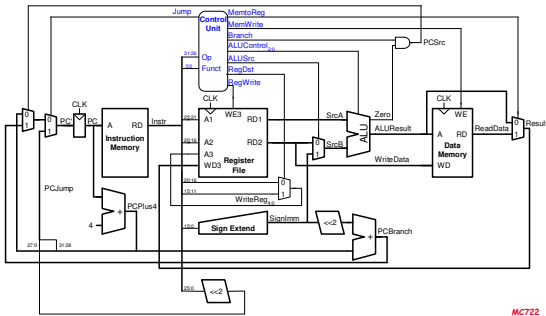
- **Decodificador Principal**

Instruction	Op _{6:0}	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	ALUOp _{2:0}	Jump
R-type	000000	1	1	0	0	0	0	10	0
lw	100011	1	0	1	0	0	1	00	0
sw	101011	0	X	1	0	1	X	00	0
beq	000100	0	X	0	1	0	X	01	0
addi	001000	1	0	1	0	0	0	00	0
j	000100	0	X	X	X	0	X	XX	1

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Processador MIPS Single-Cycle

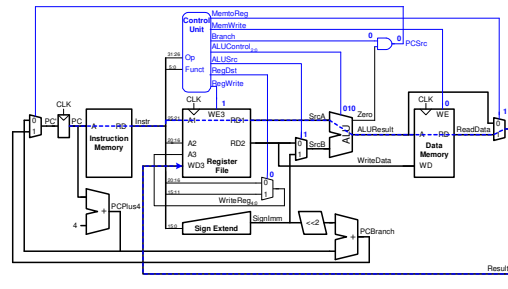
- **Desempenho: Quão rápido é o processador?**



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Processador MIPS Single-Cycle

- **O cycle time é limitado pelo caminho crítico: lw**



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Processador MIPS Single-Cycle

- **Caminho crítico**

$$T_c = t_{pcq_pc} + t_{mem} + \max(t_{Rfread}, t_{sextr}) + t_{mux} + t_{ALU} + t_{mem} + t_{mux} + t_{Rfsetup}$$

- **Na maioria das implementações os caminhos limitantes são: memória, ALU, register file. Assim,**

$$T_c = t_{pcq_pc} + 2t_{mem} + t_{Rfread} + 2t_{mux} + t_{ALU} + t_{Rfsetup}$$

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Processador MIPS Single-Cycle

Element	Parameter	Delay (ps)
Register clock-to-Q	t_{pcq_pc}	30
Register setup	t_{setup}	20
Multiplexer	t_{mux}	25
ALU	t_{ALU}	200
Memory read	t_{mem}	250
Register file read	t_{Rfread}	150
Register file setup	$t_{Rfsetup}$	20

$$T_c = t_{pcq_pc} + 2t_{mem} + t_{Rfread} + 2t_{mux} + t_{ALU} + t_{Rfsetup}$$

$$= [30 + 2(250) + 150 + 2(25) + 200 + 20] \text{ ps}$$

$$= 950 \text{ ps}$$

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Processador MIPS Single-Cycle

- Para um programa 100 bilhões de instruções executando em um processador MIPS single-cycle,

$$\begin{aligned} \text{Execution Time} &= (\# \text{ instructions})(\text{cycles/instruction})(\text{seconds/cycle}) \\ &= (100 \times 10^9)(1)(950 \times 10^{-12} \text{ s}) \\ &= 95 \text{ seconds} \end{aligned}$$

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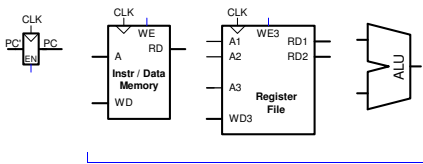
Processador MIPS Multicycle

- Datapath
- Controle

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Processador MIPS Multicycle

- Blocos Básicos



Restrição de Projeto:

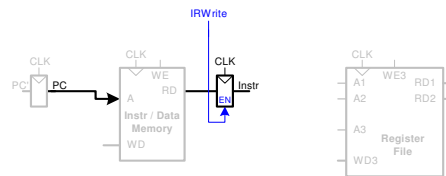
Somente 1 bloco acima pode ser usado por vez

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Processador MIPS Multicycle

- Datapath
 - datapath para o lw
 - Exemplo: lw \$s4, 27(\$t2)

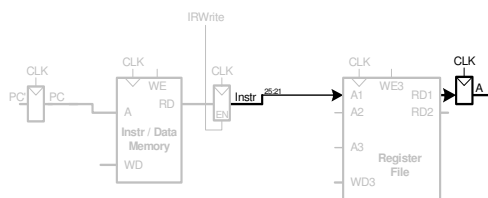
- Fetch da Instrução



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Processador MIPS Multicycle

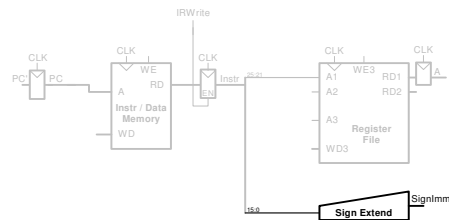
- Leitura do operando fonte do RF (rs)



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Processador MIPS Multicycle

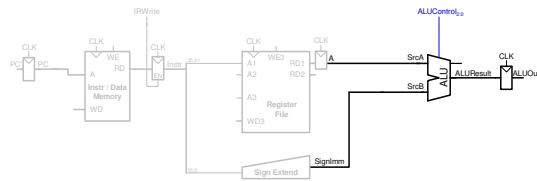
- Sign-Extend o Imediato



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Processador MIPS Multicycle

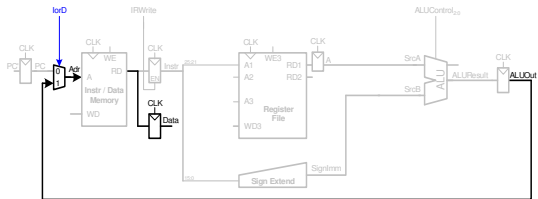
- Soma do Base Address ao Offset



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Processador MIPS Multicycle

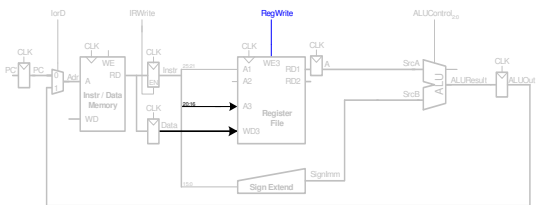
- Carga do dado a partir da Memória



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Processador MIPS Multicycle

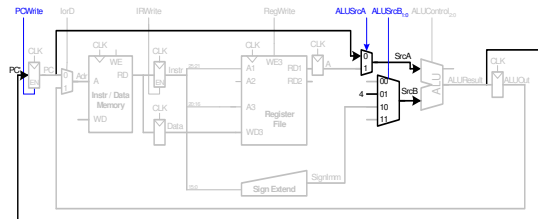
- Escrita do Dado no Register File



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Processador MIPS Multicycle

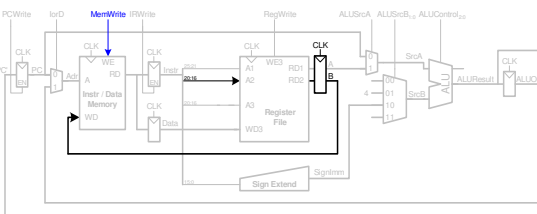
- Incremento do PC de 4



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Processador MIPS Multicycle

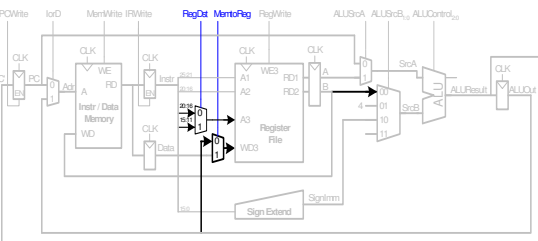
- Datapath também para sw



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Processador MIPS Multicycle

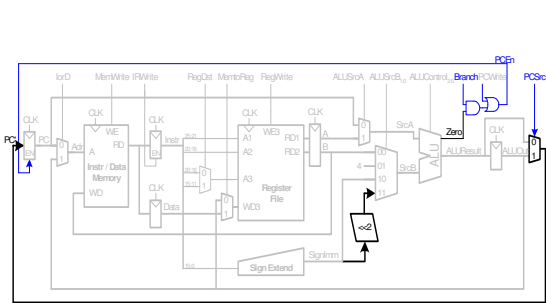
- Datapath para instruções R-Type



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Processador MIPS Multicycle

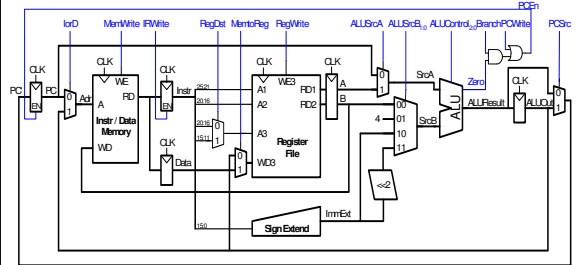
- Datapath para beq



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Processador MIPS Multicycle

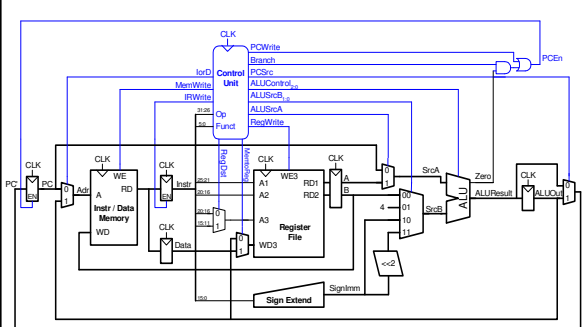
- Datapath para o Processor Multicycle



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Processador MIPS Multicycle

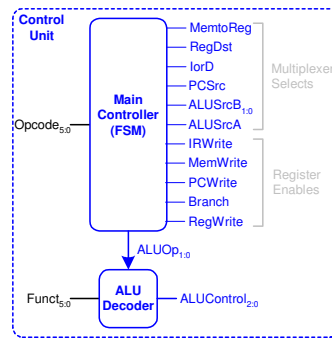
- Controle para o Processor Multicycle



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Processador MIPS Multicycle

- Unidade de controle



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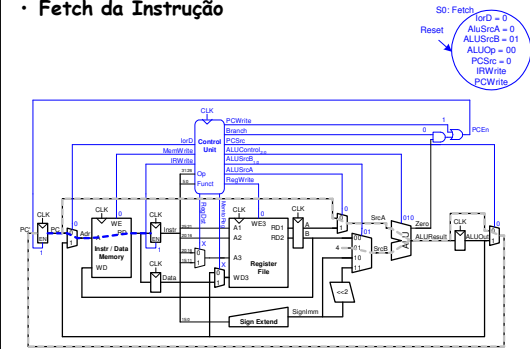
Processador MIPS Multicycle

- Unidade de Controle
 - Finite State Machine
 - Diagrama de transição de estados para 1w

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Processador MIPS Multicycle

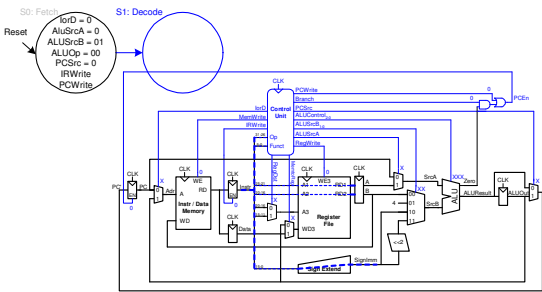
- Fetch da Instrução



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Processador MIPS Multicycle

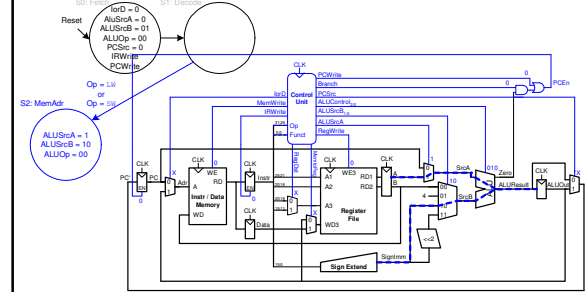
• Decodificação da Instrução



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Processador MIPS Multicycle

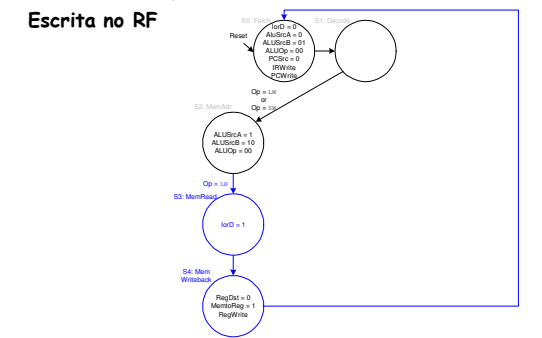
• Cálculo do endereço efetivo



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Processador MIPS Multicycle

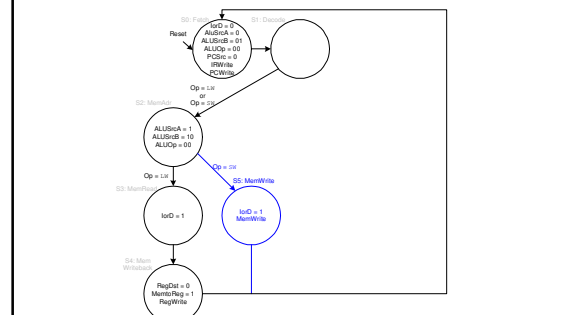
• Leitura da Memória e Escrita no RF



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Processador MIPS Multicycle

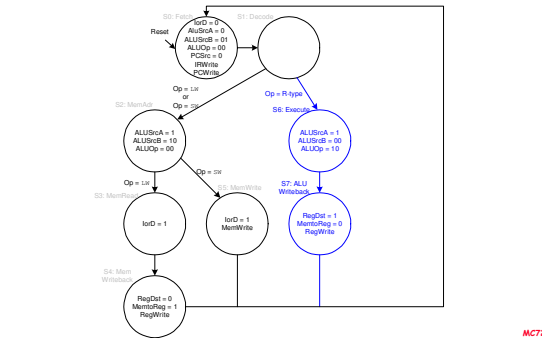
• Diagrama de transição de estados para sw



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Processador MIPS Multicycle

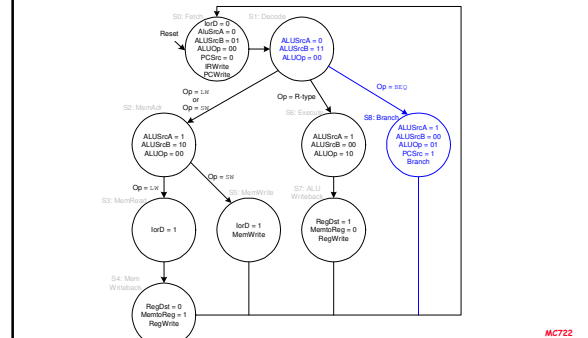
• Diagrama de transição de estados para R-type



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Processador MIPS Multicycle

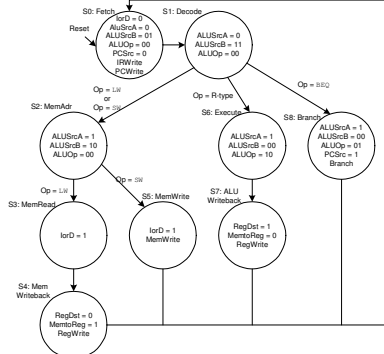
• Diagrama de transição de estados para beq



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Processador MIPS Multicycle

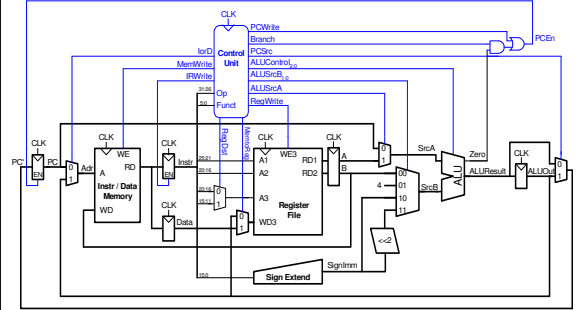
FSM de Controle



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Processador MIPS Multicycle

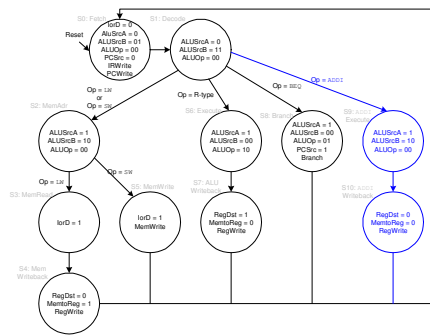
Extendendo a Funcionalidade para addi



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Processador MIPS Multicycle

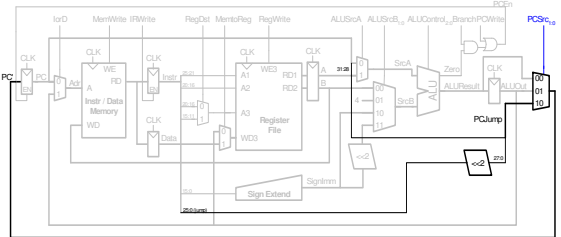
FSM de Controle para addi



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Processador MIPS Multicycle

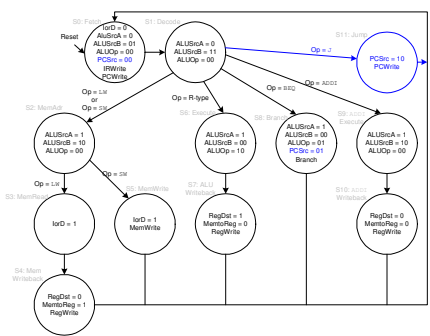
Extendendo a Funcionalidade para j



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Processador MIPS Multicycle

FSM de Controle para j



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Processador MIPS Multicycle

Desempenho: Quão rápido é o processador?

- Instruções gastam números diferentes de ciclos:
 - 3 ciclos: beq, j
 - 4 ciclos: R-Type, sw, addi
 - 5 ciclos: lw
- O CPI deve ser a média ponderada
- SPECINT2000 benchmark:
 - 25% loads
 - 10% stores
 - 11% branches
 - 2% jumps
 - 52% R-type

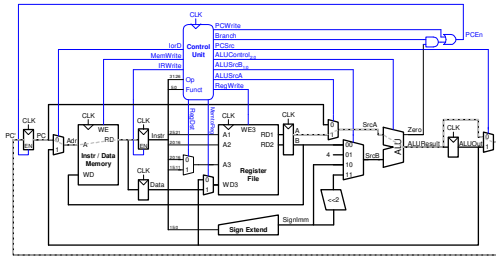
$$\text{Average CPI} = (0.11 + 0.2)(3) + (0.52 + 0.10)(4) + (0.25)(5) = 4.12$$

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Processador MIPS Multicycle

• Caminho Crítico

$$T_c = t_{pcq_PC} + t_{mux} + \max(t_{ALU} + t_{mux}, t_{mem}) + t_{setup}$$



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Processador MIPS Multicycle

Element	Parameter	Delay (ps)
Register clock-to-Q	t_{pcq_PC}	30
Register setup	t_{setup}	20
Multiplexer	t_{mux}	25
ALU	t_{ALU}	200
Memory read	t_{mem}	250
Register file read	t_{RFread}	150
Register file setup	$t_{RFsetup}$	20

$$\begin{aligned} T_c &= t_{pcq_PC} + t_{mux} + \max(t_{ALU} + t_{mux}, t_{mem}) + t_{setup} \\ &= t_{pcq_PC} + t_{mux} + t_{mem} + t_{setup} \\ &= [30 + 25 + 250 + 20] \text{ ps} \\ &= 325 \text{ ps} \end{aligned}$$

MC722
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Processador MIPS Multicycle

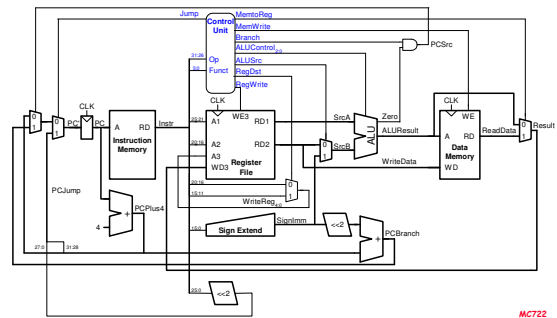
- Para um programa que executa 100 bilhões de instruções em um MIPS multicycle,
- CPI = 4.12
- $T_c = 325 \text{ ps}$

$$\begin{aligned} \text{Execution Time} &= (\# \text{ instructions}) \times \text{CPI} \times T_c \\ &= (100 \times 10^9)(4.12)(325 \times 10^{-12}) \\ &= 133.9 \text{ seconds} \end{aligned}$$

- Ele é mais lento do que o MIPS single-cycle (95 segundos). Por que?
 - Os passos não tem o mesmo tamanho
 - Overhead do seqüenciamento de cada passo ($t_{pcq} + t_{setup} = 50 \text{ ps}$)

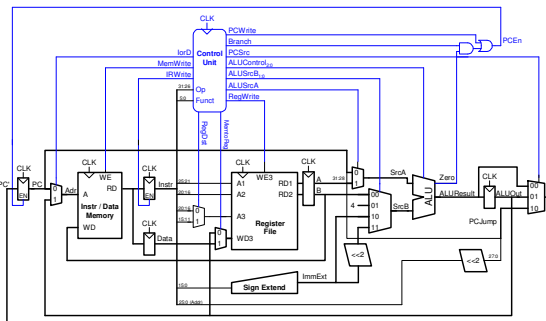
MC722
3.69

Revisão: Processador MIPS Single Cycle



MC722
3.70

Revisão: Processador MIPS Multicycle



MC722
3.71