MC542

Organização de Computadores
Teoria e Prática

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MC542

Circuitos Lógicos

Projeto de Circuitos Seqüenciais

"DDCA" - (Capítulo 3)
"FDL" - (Capítulo 7)

Projeto de Circuitos Seqüenciais
Sumário

Introdução

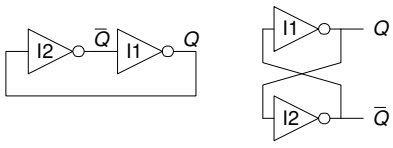
- As saídas de um circuito seqüencial dependem dos valores presente e passados de suas entradas.
- Lógica seqüencial possue memória.
- Algumas definições:
  - Estado (State): conjunto de informações a cerca do circuito necessárias para se prever o seu comportamento futuro.
  - Latches e flip-flops: elementos de estado que armazenam um bit
  - Circuitos seqüencias Síncronos: circuito combinacional seguido de um banco de flip-flops

Elementos de Estados

- O estado de um circuito determina o seu comportamento futuro
- Elementos de Estado armazenam o estado
  - Circuito bi-estável
  - Latch SR
  - Latch D
  - Flip-flop D
    - » Outros tipos de flip-flops
      - JK
      - T
      - SR

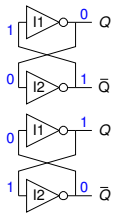
Circuito Bi-estável

- Bloco Fundamental para a construção dos outros elementos de estado
- Duas saídas: Q, $\overline{Q}$
- Sem entradas.



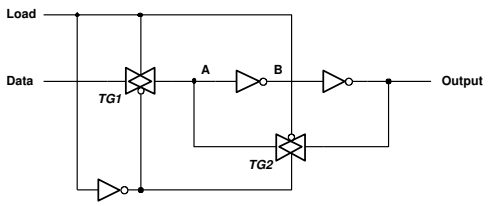
Circuito Bi-estável: Comportamento

- Considere os dois posíveis casos:
  - $Q = 0$: então $\bar{Q} = 1$ and $Q = 0$
  - $Q = 1$: então $\bar{Q} = 0$ and $Q = 1$



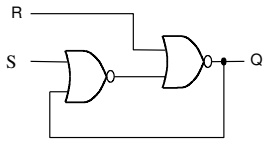
- O circuito bi-estável armazena 1 bit do estado na variável, Q (ou Q̄)
- Porém não há entrada para controle do estado

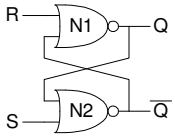
Elemento de Memória com Controle



SR Latch

- Latch Set/Reset (Latch SR)
- Definições
  - Set: Saída igual a 1
  - Reset: saída igual a 0
- Quando a entrada set, S, é 1 (e $R = 0$), $Q = 1$
- Quando a entrada reset, R, é 1 (e $S = 0$), $Q = 0$





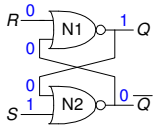
- Qual a tabela verdade?

SR Latch

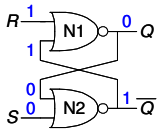
- Considere os quatro casos possíveis:
  - $S = 1$, $R = 0$
  - $S = 0$, $R = 1$
  - $S = 0$, $R = 0$
  - $S = 1$, $R = 1$

SR Latch

- $S = 1$, $R = 0$: then $Q = 1$ and $\bar{Q} = 0$

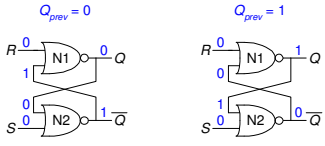


- $S = 0$, $R = 1$: then $Q = 0$ and $\bar{Q} = 1$

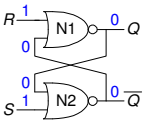


SR Latch

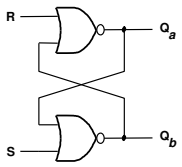
- $S = 0$, $R = 0$: então $Q = Q_{prev}$ e $\bar{Q} = \overline{Q_{prev}}$ (memória!)



- $S = 1$, $R = 1$: então $Q = 0$ e $\bar{Q} = 0$ (estado invalido: $\bar{Q} \neq$ NOT Q)



SR Latch



S	R	Q_a	Q_b	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

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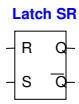
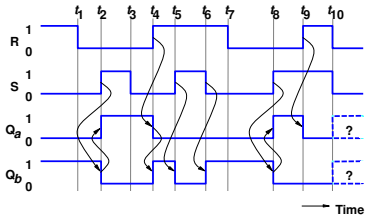
SR Latch

Latch SR





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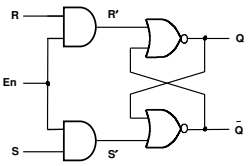
Latch SR com Enable



En	S	R	Q(*t* + 1)
0	x	x	Q(*t*) (no change)
1	0	0	Q(*t*) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

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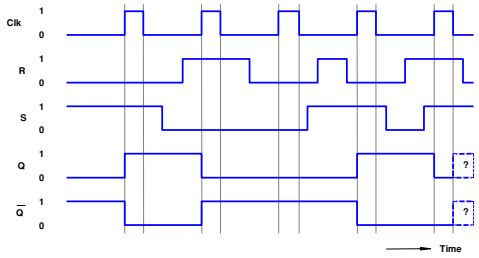
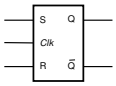
Latch SR com Enable





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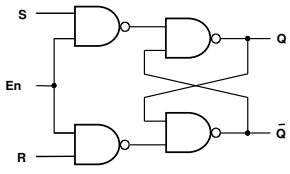
Latch SR com Nand



Qual a tabela verdade?

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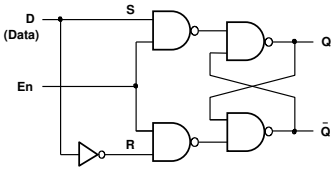
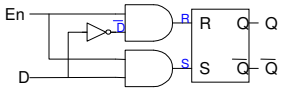
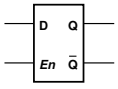
Latch D



En	D	Q(*t* + 1)
0	x	Q(*t*)
1	0	0
1	1	1





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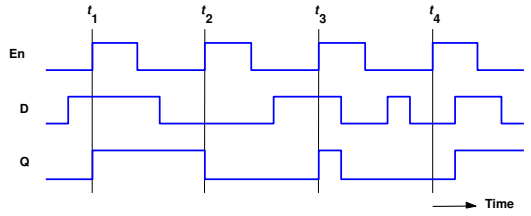
Latch D



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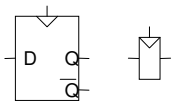
Flip-Flop D

- Duas entradas: *CLK*, *D*
- *Q* só muda na borda (subida ou decida) do *CLK*
- O flip-flop "samples" *D* na borda do *CLK*
- O flip-flop é chamado de dispositivo *edge-triggered* devido a ser ativo na borda do clock

Flip-Flop D



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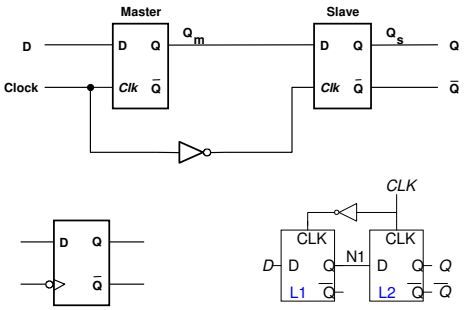
Flip-Flop D Mestre-Escravo



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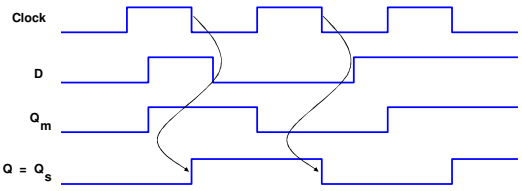
Flip-Flop D Mestre-Escravo



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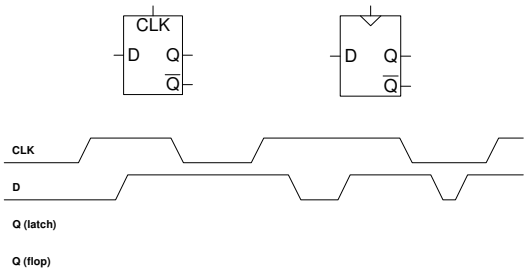
Flip-Flop D vs. Latch D



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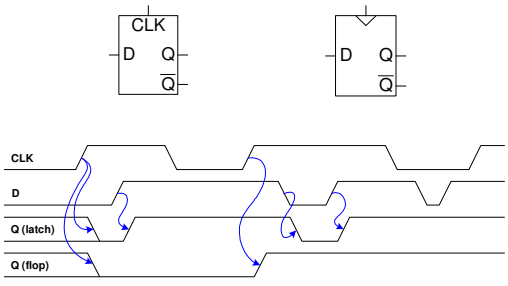
Flip-Flop D vs. Latch D



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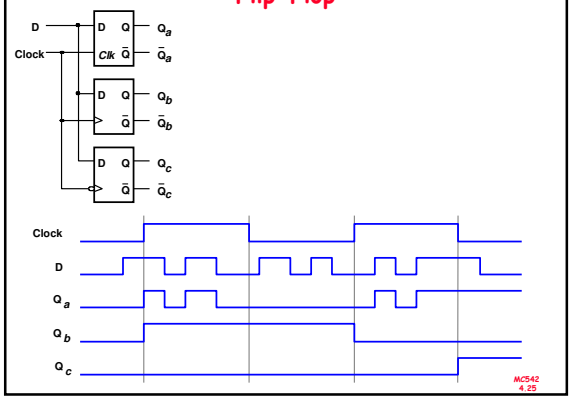
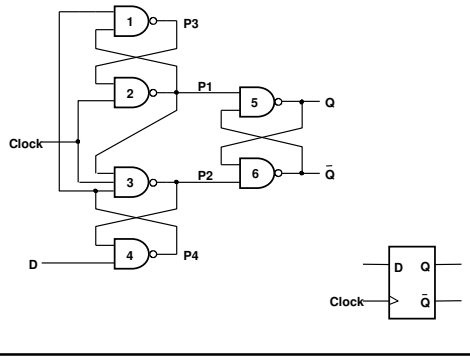
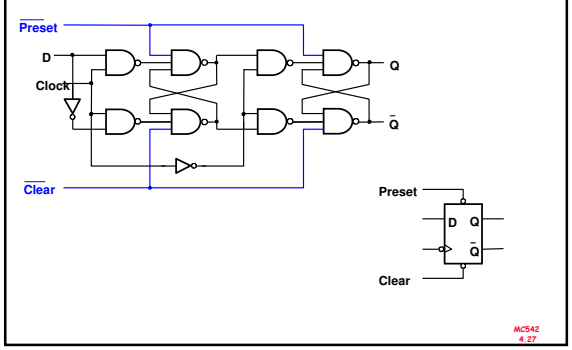
Flip-Flop



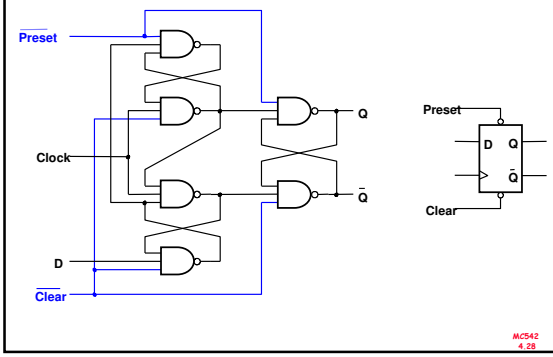
Flip-Flop D Sensível à Borda de Subida



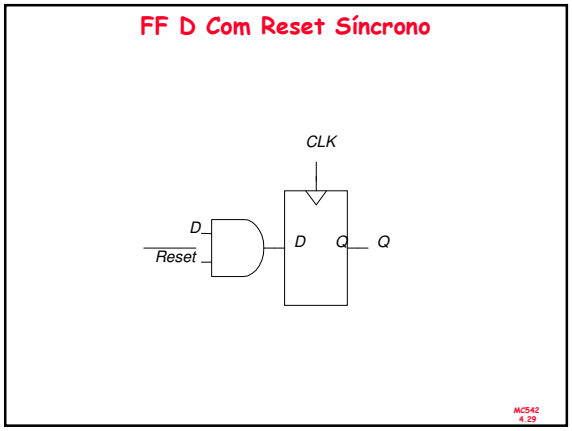
FF D Mestre-Escravo com Preste e Clear Assíncronos



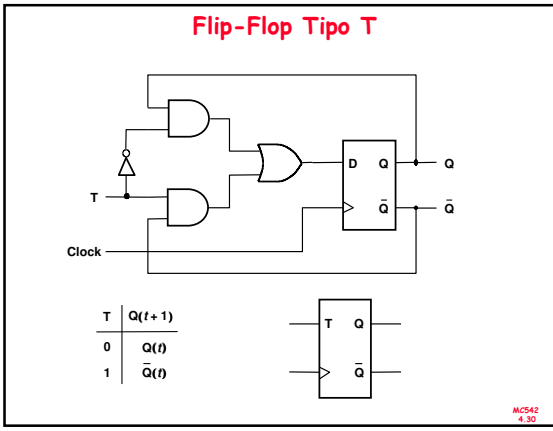
FF D Sensível à Borda com Preste e Clear Assíncrono



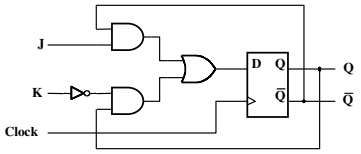
FF D Com Reset Síncrono



Flip-Flop Tipo T



Flip-Flop Tipo JK



J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q̄(t)

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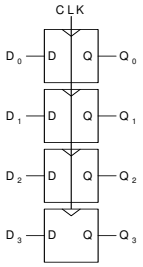
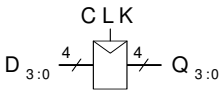
Registradores

- Conjunto de elementos de memória (flip-flops) utilizados para armazenar n bits.
- Utilizam em comum os sinais de clock e controle





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Shift Register

Apresenta o seuinte comportamento:

	In	Q_1	Q_2	Q_3	Q_4 = Out
t_0	1	0	0	0	0
t_1	0	1	0	0	0
t_2	1	0	1	0	0
t_3	1	1	0	1	0
t_4	1	1	1	0	1
t_5	0	1	1	1	0
t_6	0	0	1	1	1
t_7	0	0	0	1	1

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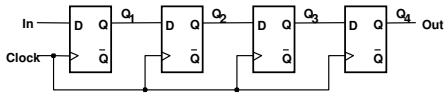
Shift Register



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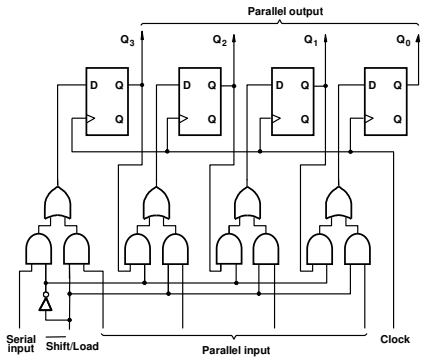
Shift Register com Carga Paralela



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Shift Register Universal

- Entrada Serial
  - Deslocamento a Esquerda
  - Deslocamento a Direita
- Carga Paralela
- Saída Paralela

- Exercício: Desenhe o Diagrama do Shift Register Universal de 4 bits.

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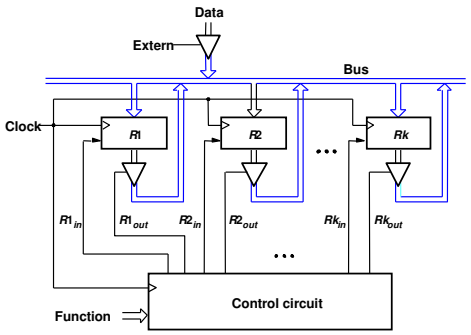
Registradores em um Barramento



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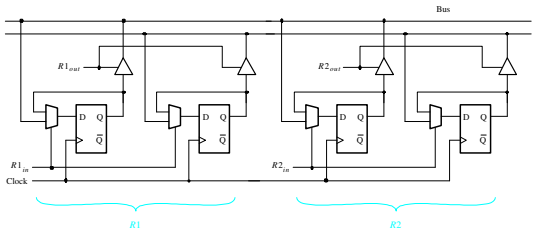
Registradores em um Barramento



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Contadores

- Assíncronos
- Síncronos

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Contadores

Contador Binário

	clk	Q_2	Q_1	Q_0
t_0	↑	0	0	0
t_1	↑	0	0	1
t_2	↑	0	1	0
t_3	↑	0	1	1
t_4	↑	1	0	0
t_5	↑	1	0	1
t_6	↑	1	1	0
t_7	↑	1	1	1

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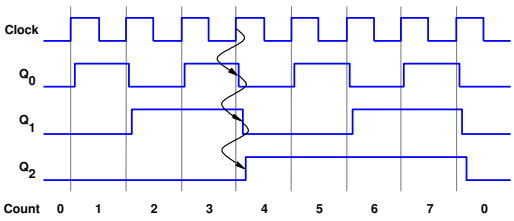
Contador Binário – FF Tipo T



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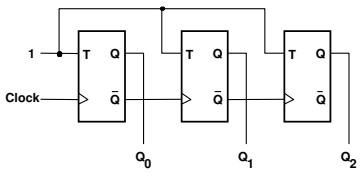
Contador Binário – FF Tipo T



Contador Binário Assíncrono (up-counter)

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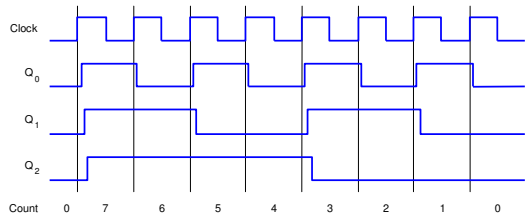
Contador Binário – FF Tipo T (Down-Counter)



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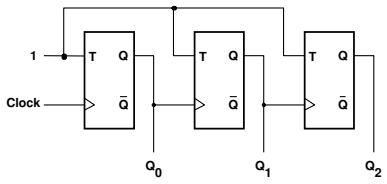
Contador Binário – FF Tipo T (Down-Counter)



Contador Binário Assíncrono (down-counter)

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Contadores Síncronos

Clock cycle	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Q_1 changes

Q_2 changes

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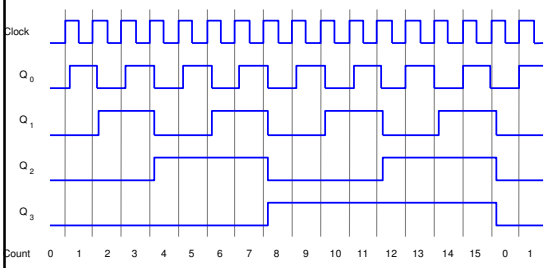
Contador Binário Síncrono



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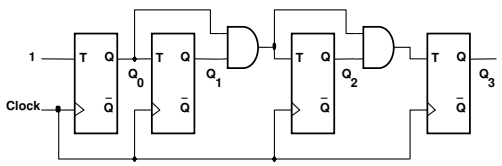
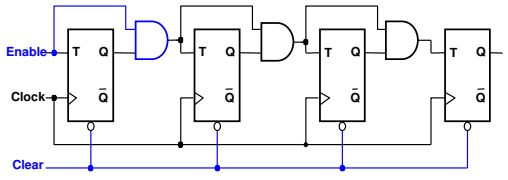
Contador Binário Síncrono



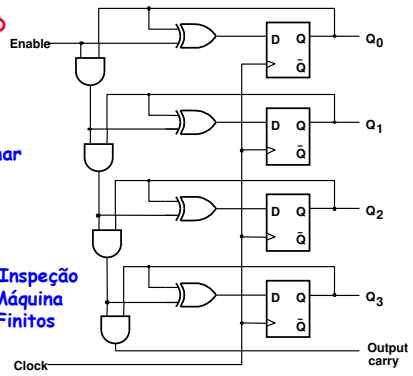
MC542 4.47

Contador Binário Síncrono com Enable e Clear



MC542 4.48

Contador de 4 bits com FF D

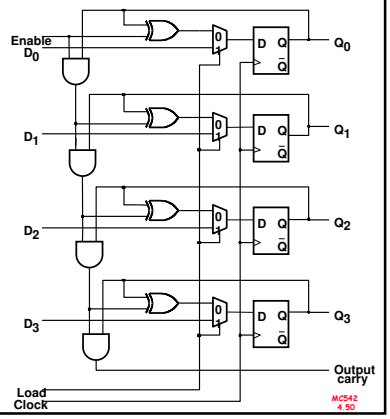


Como determinar as funções de exitação de cada FF?

1. Projeto por Inspeção
2. Projeto de Máquina de Estados Finitos (FSM)

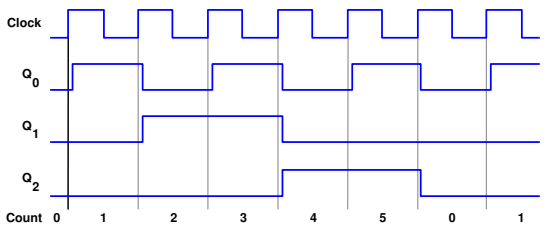
MC542 4.49

Contador de 4 bits com FF D com Carga Paralela



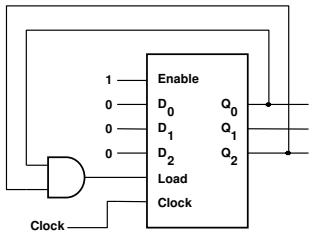
MC542 4.50

Contador Módulo (exemplo:. Módulo 6)



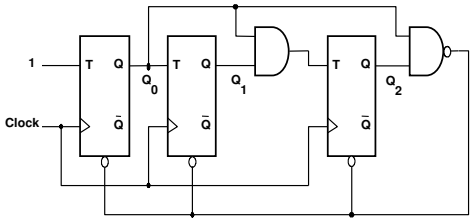
MC542 4.51

Contador Módulo (exemplo: Módulo 6)



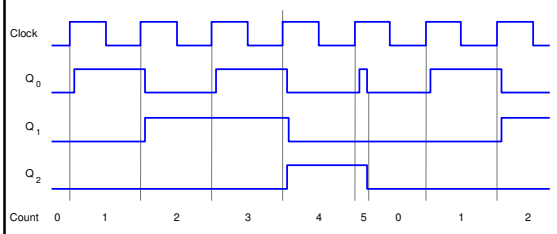
MC542 4.52

Contador Módulo 6 com Reset Assíncrono



MC542 4.53

Contador Módulo 6 com Reset Assíncrono



MC542 4.54