MC542

Organização de Computadores
Teoria e Prática

2007

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MC542

Circuitos Lógicos

Portas Lógicas, Tecnologia

"DDCA" - (Capítulo 1)
"FDL" - (Capítulo 3)

Portas Lógicas, Tecnologia
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  - Funções Complexas
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Portas Lógicas, Tecnologia
Sumário

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- Portas Lógicas com NMOS
- Portas Lógicas com CMOS
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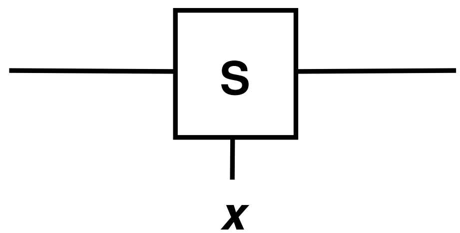
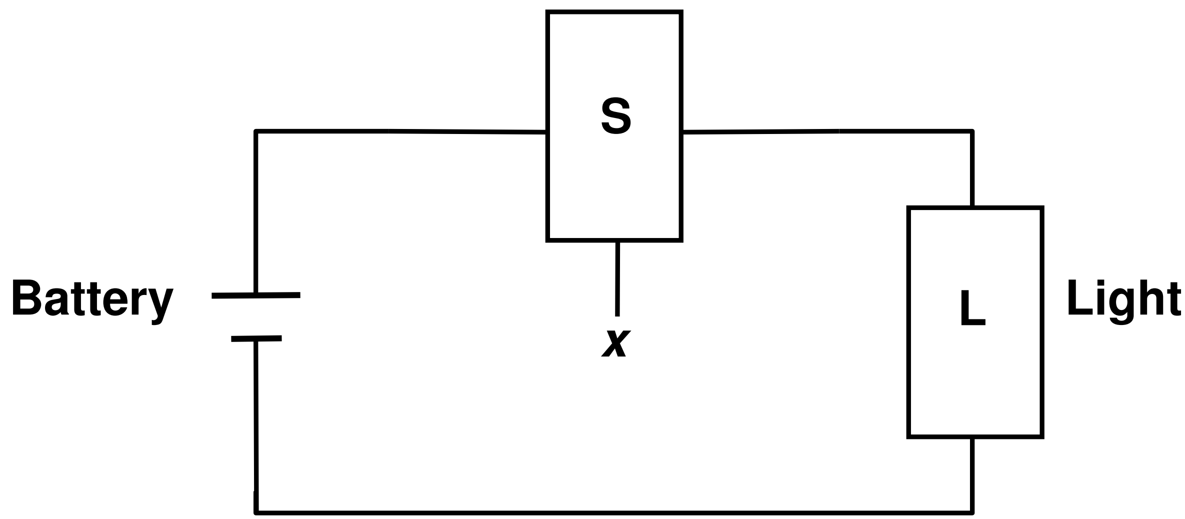
- Tri-state

Variáveis e Funções

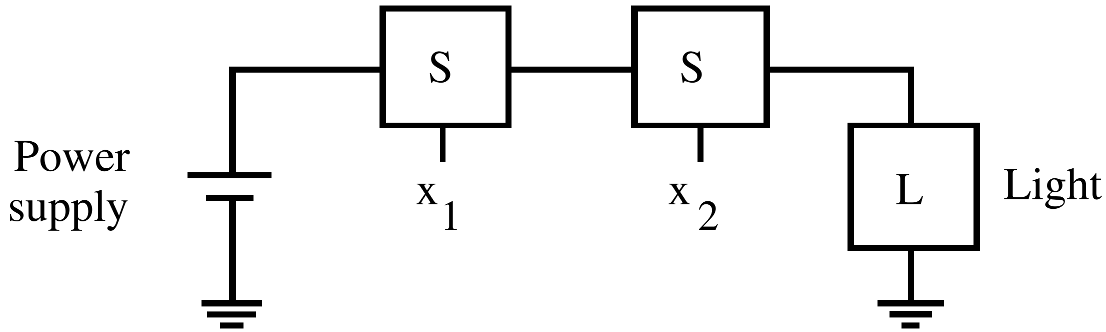
Analogia com chaves controladas



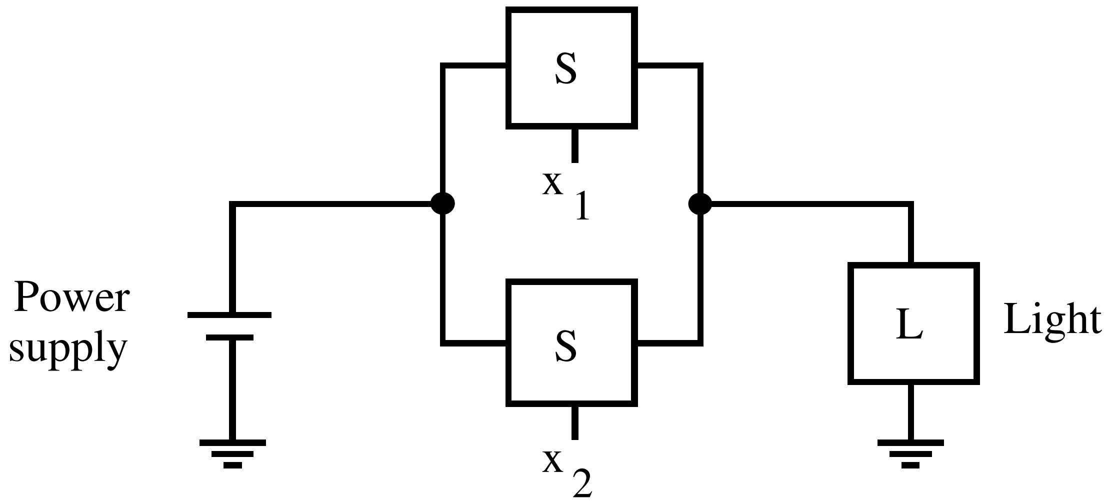
Variáveis e Funções



Variáveis e Funções - Funções Simples
AND e OR

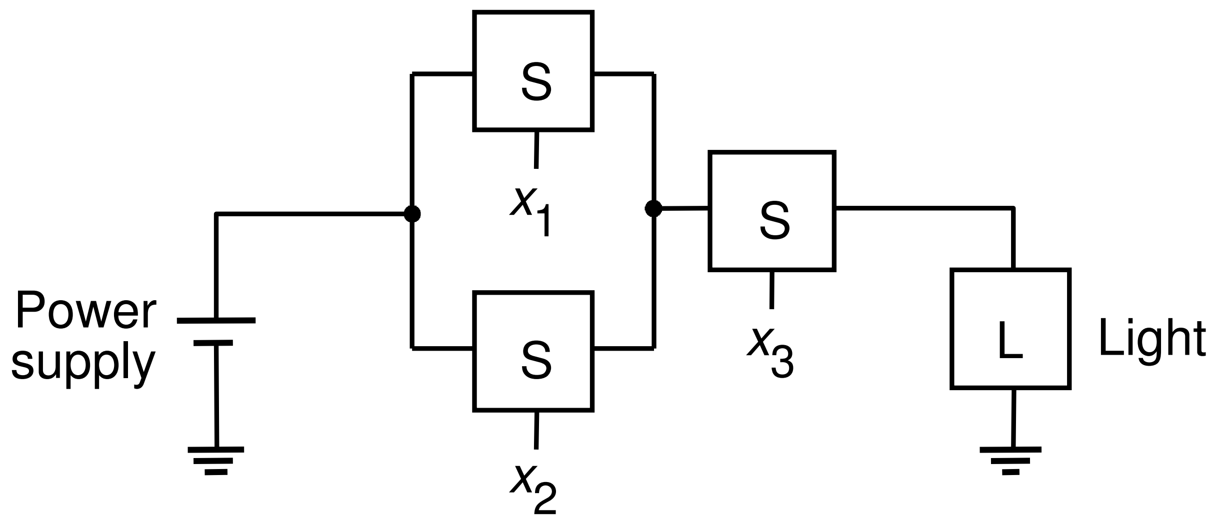


Função lógica AND



Função lógica OR

Variáveis e Funções - Funções Complexas



Arranjo serie/paralelo

Variáveis e Funções
NOT

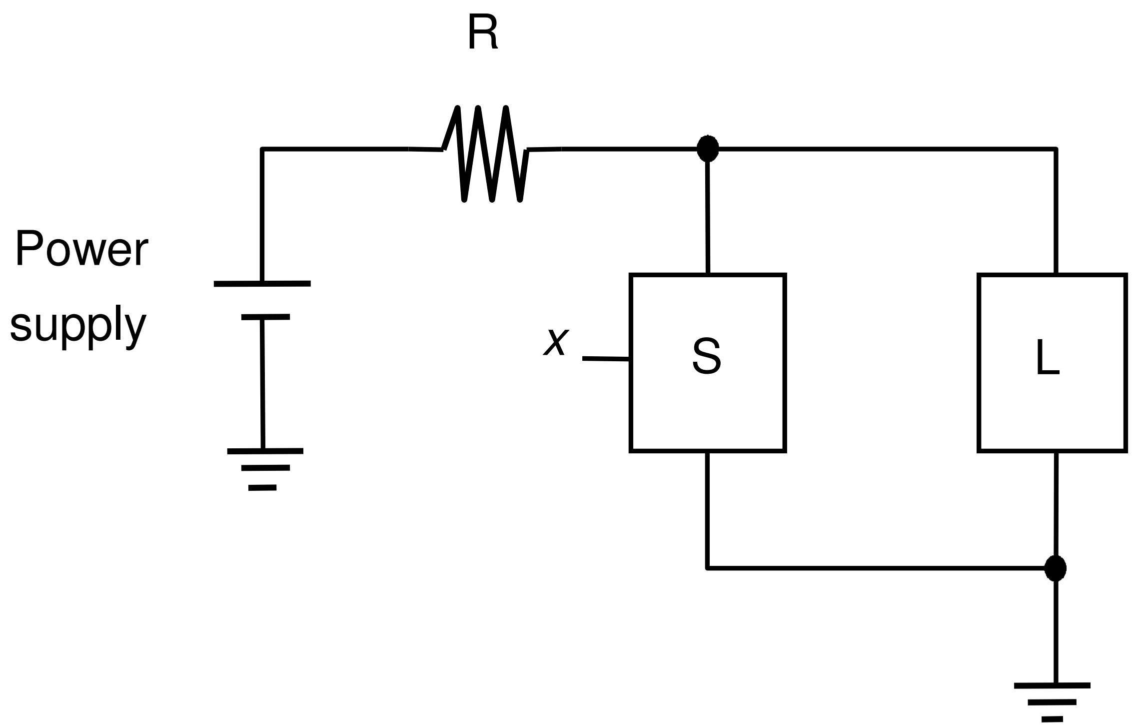


Tabela Verdade

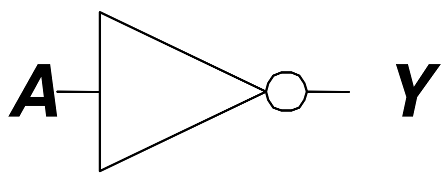
x_1	x_2	$x_1 \cdot x_2$	$x_1 + x_2$
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1
		AND	OR

Tabela Verdade

x_1	x_2	x_3	$x_1 \cdot x_2 \cdot x_3$	$x_1 + x_2 + x_3$
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Portas Lógicas: Uma Entrada (ou Gates)

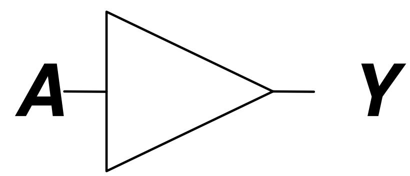
NOT



$$Y = \overline{A}$$

A	Y
0	1
1	0

BUF

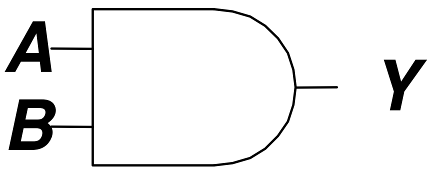


$$Y = A$$

A	Y
0	0
1	1

Portas Lógicas: Duas Entradas

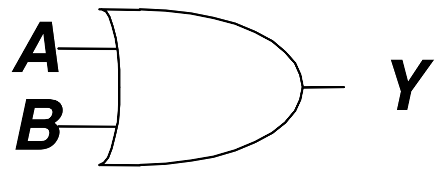
AND



$$Y = AB$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR

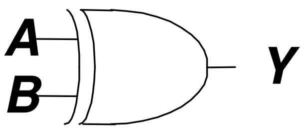


$$Y = A + B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Portas Lógicas: Duas Entradas

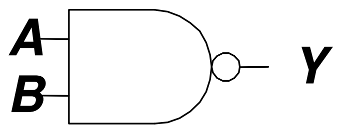
XOR



$$Y = A \oplus B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

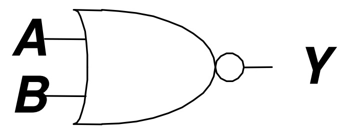
NAND



$$Y = \overline{AB}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

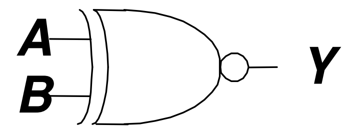
NOR



$$Y = \overline{A + B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XNOR

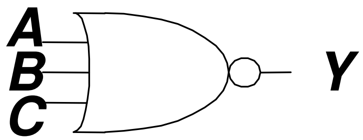


$$Y = \overline{A \oplus B}$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

Portas Lógicas: Múltiplas Entradas

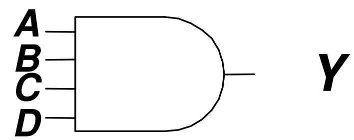
NOR3



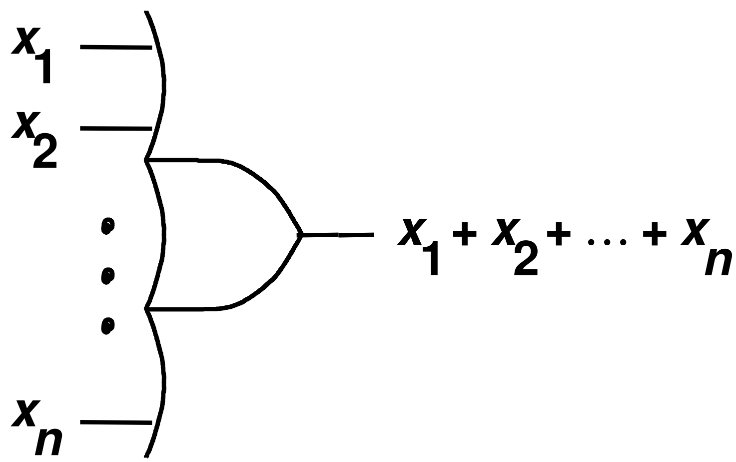
$$Y = \overline{A+B+C}$$

A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

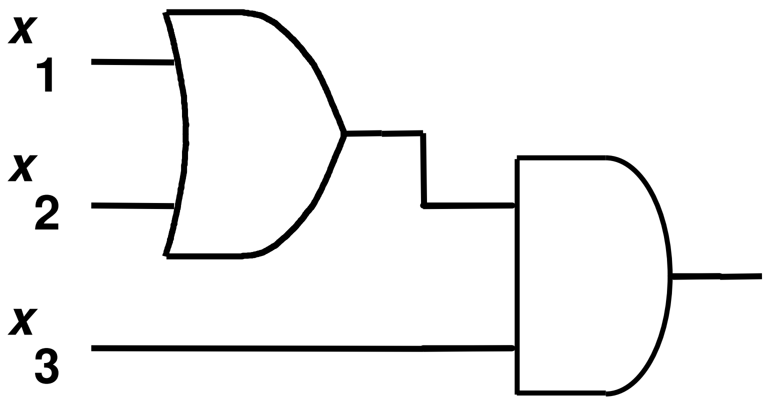
AND4



$$Y = ABCD$$



Rede Lógica



$f = (x_1 + x_2) \cdot x_3$

Rede de portas
Circuito lógico

Níveis Lógicos

- Define as voltagens para representar o 1 e o 0

- Exemplo:
  - 0 : terra ou 0 volts
  - 1 : V_{DD} ou 5 volts

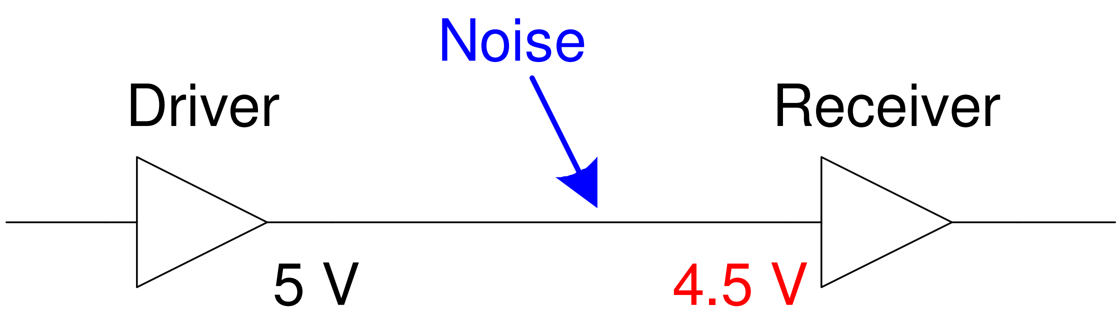
- Qual o valor produzido por uma porta (gate)?

- Se produzir 4.99 volts? Isso é um 0 ou um 1?

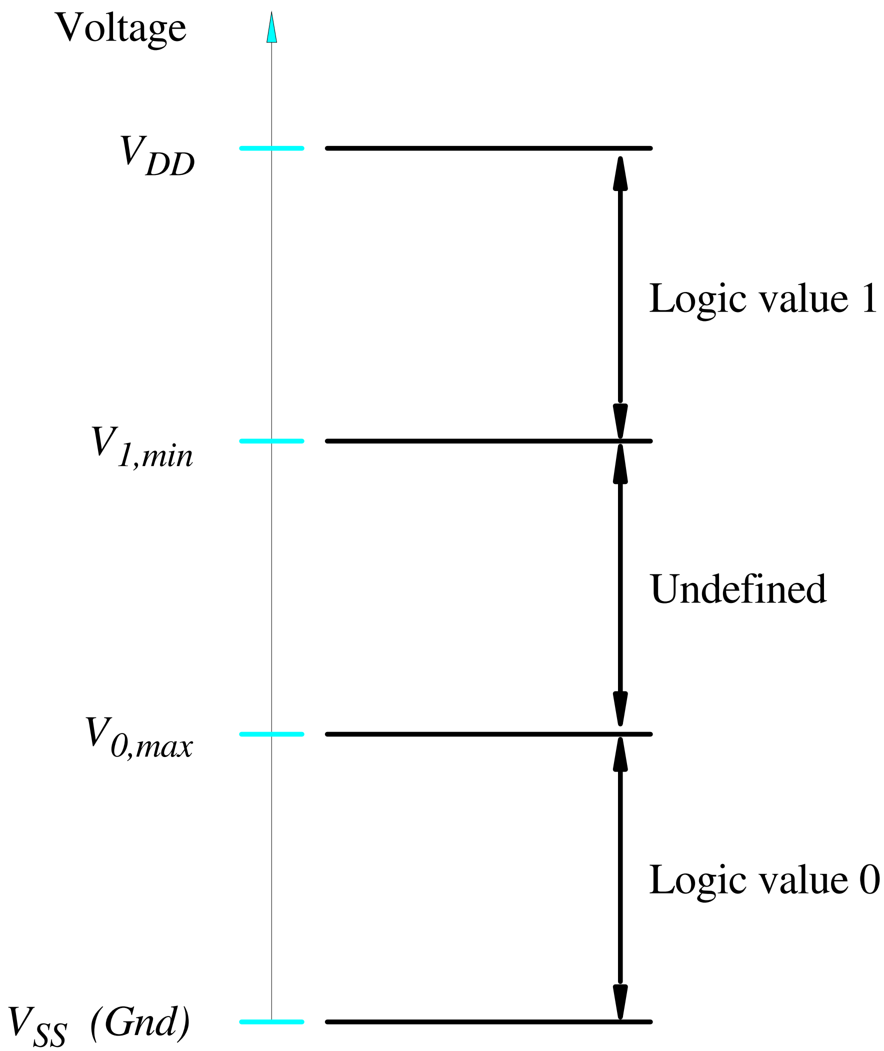
- E se 3.2 volts?

Níveis Lógico

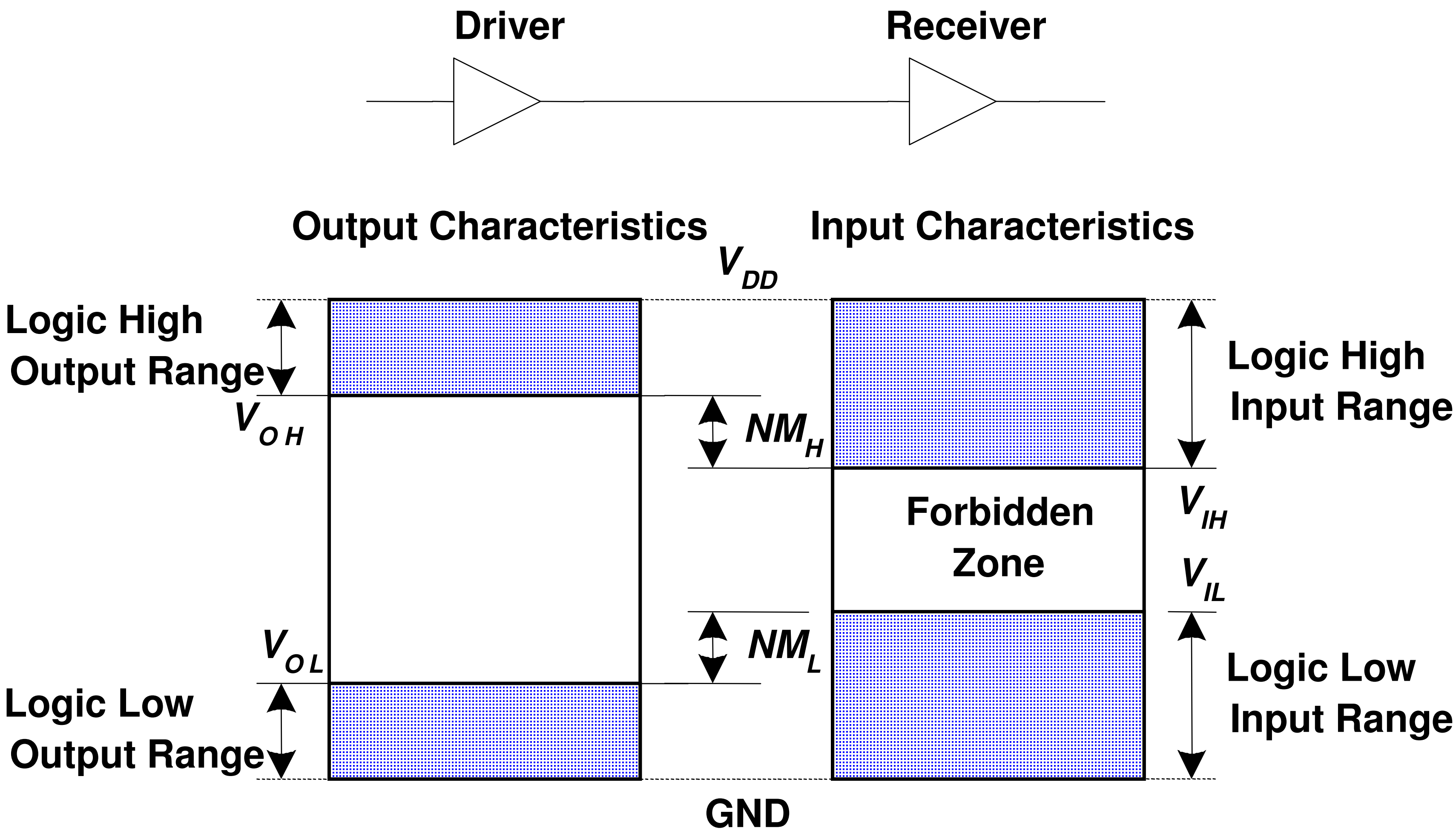
- Define-se intervalos de voltagens para representar o 1 e o 0
- Define-se diferentes intervalos para saídas e entradas para permitir tolerância a ruídos
- Ruído é qualquer coisa que degrada o sinal



Níveis Lógico



Níveis Lógicos: Margem de Ruído

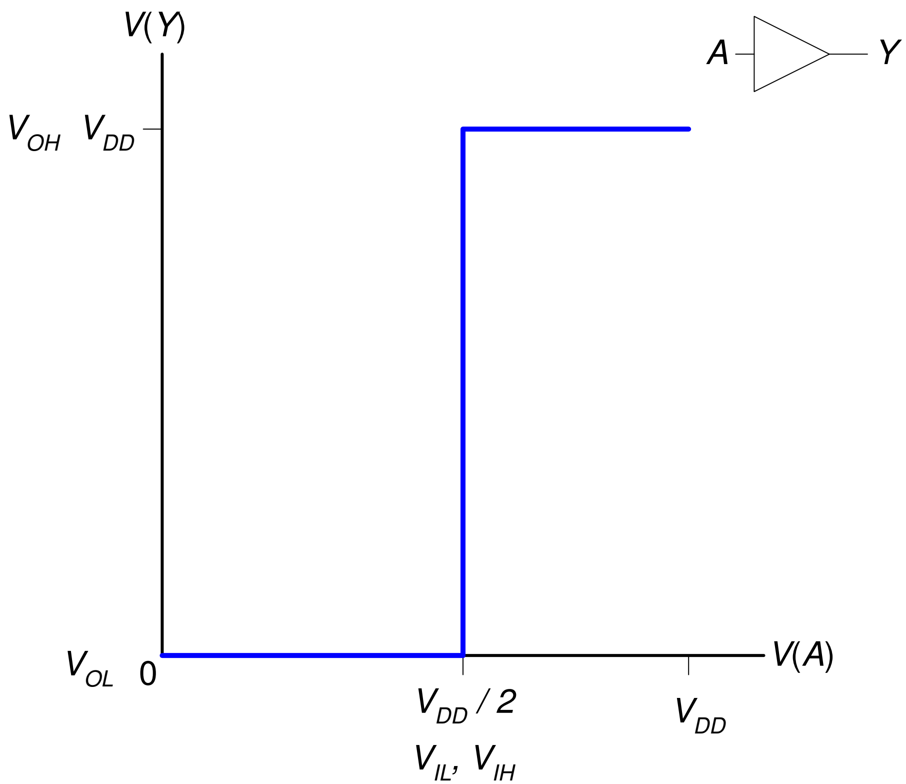


$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

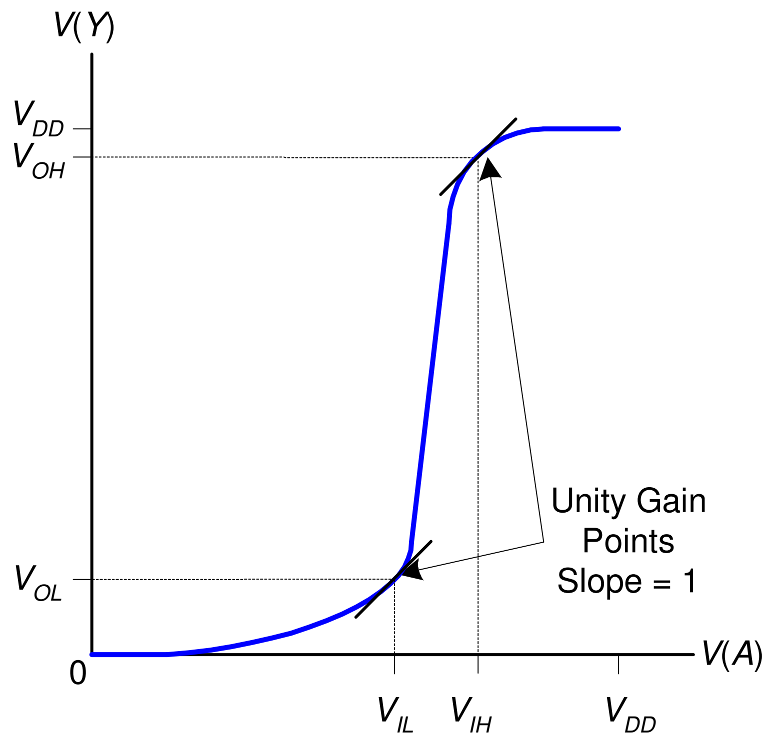
Característica de Transferência DC

Ideal Buffer:



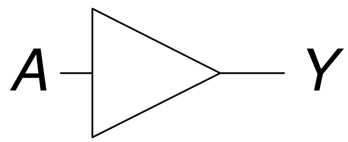
$NM_H = NM_L = V_{DD}/2$

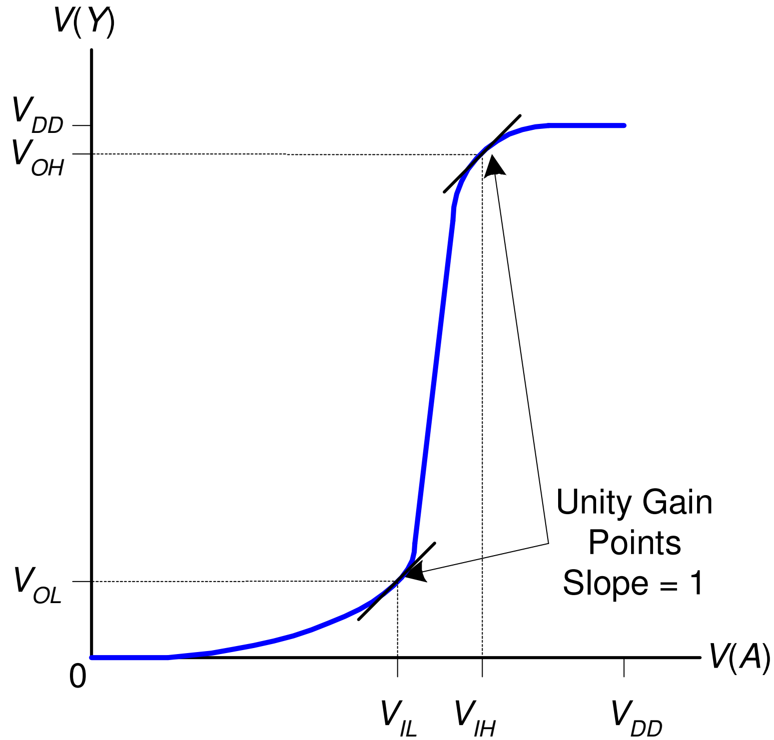
Real Buffer:

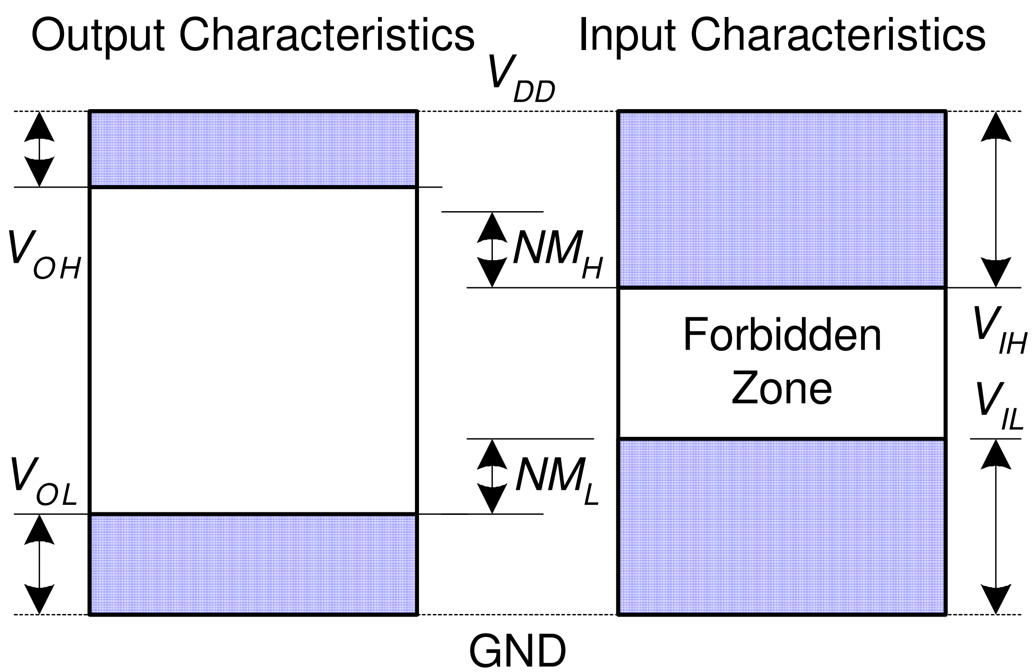


$NM_H, NM_L < V_{DD}/2$

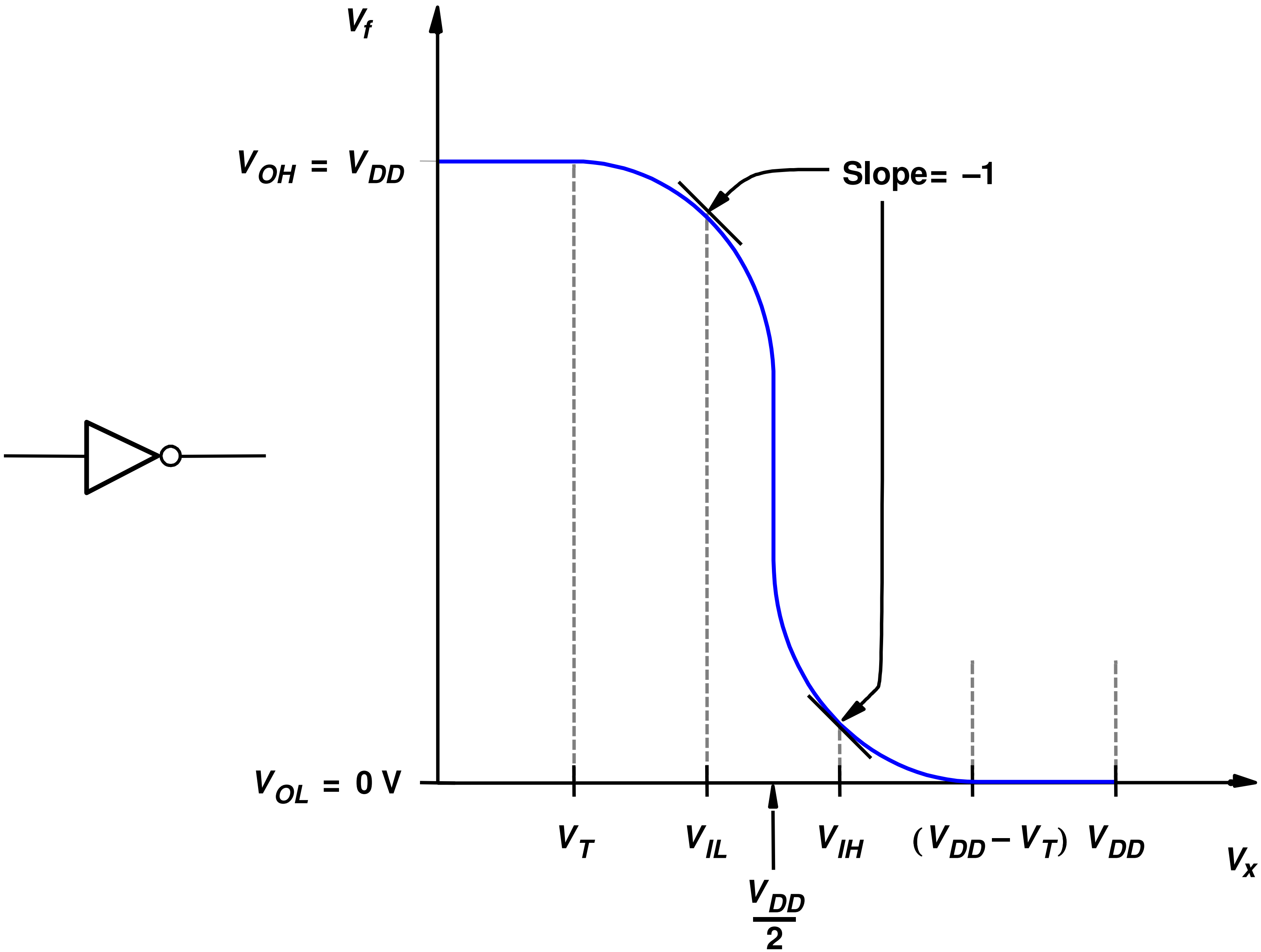
Característica de Transferência DC







Característica de Transferência DC

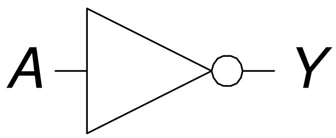


Família Lógicas

Logic Family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (4.75 - 5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5 - 6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3 - 3.6)	0.8	2.0	0.4	2.4
LVCMOS	3.3 (3 - 3.6)	0.9	1.8	0.36	2.7

Como Construir as Portas Lógicas

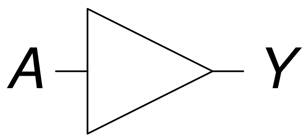
NOT



$Y = \overline{A}$

A	Y
0	1
1	0

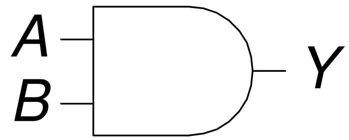
BUF



$Y = A$

A	Y
0	0
1	1

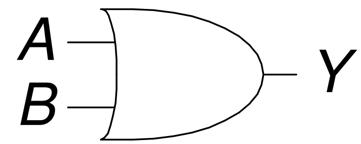
AND



$Y = AB$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR



$Y = A + B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

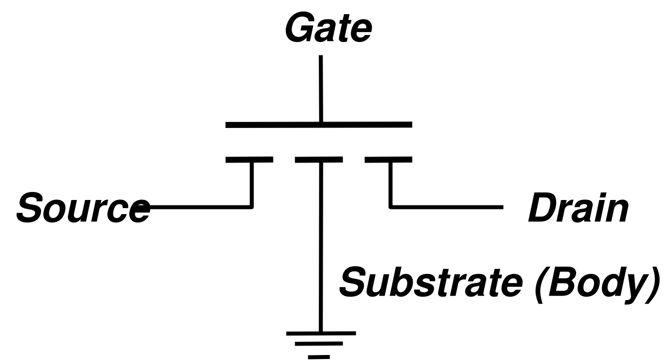
Transistores!

Transistor como Chave

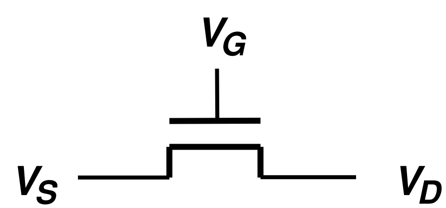
MOSFET: Metal oxide semiconductor field-effect transistor

MOSFET: NMOS e PMOS

A simple switch controlled by the input x



NMOS transistor

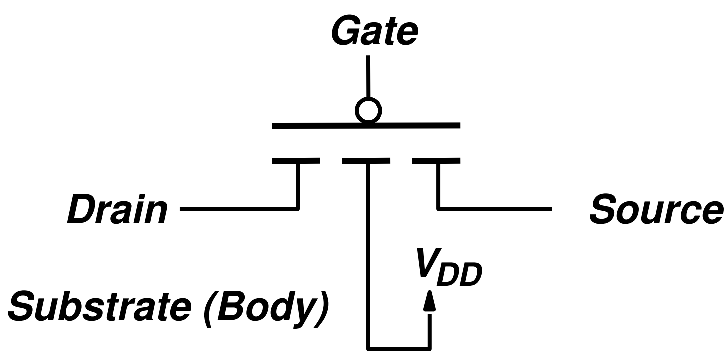


Simplified symbol for an NMOS transistor

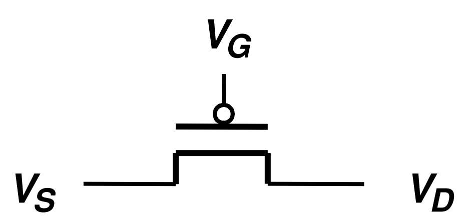
NMOS transistor as a switch

Transistor como Chave

A switch with the opposite behavior of Figure 3.2



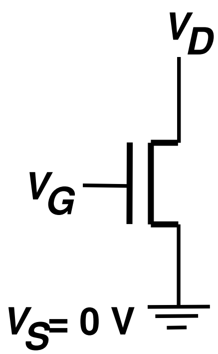
PMOS transistor



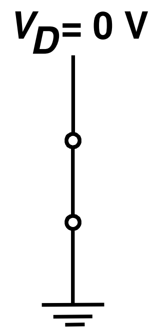
Simplified symbol for an PMOS transistor

PMOS transistor as a switch

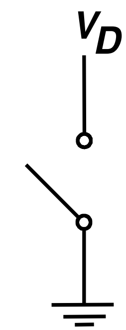
Comportamento dos Transistores NMOS e PMOS em Circuitos



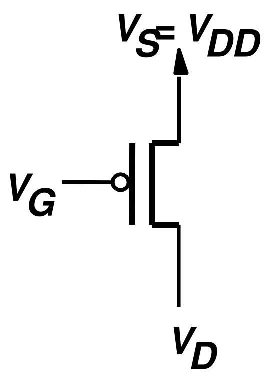
Transistor NMOS



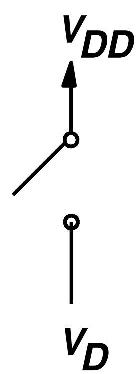
Closed switch
when $V_G = V_{DD}$



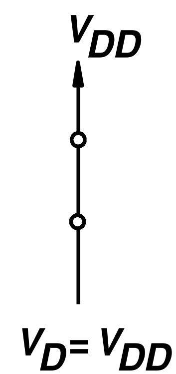
Open switch
when $V_G = 0$ V



Transistor PMOS



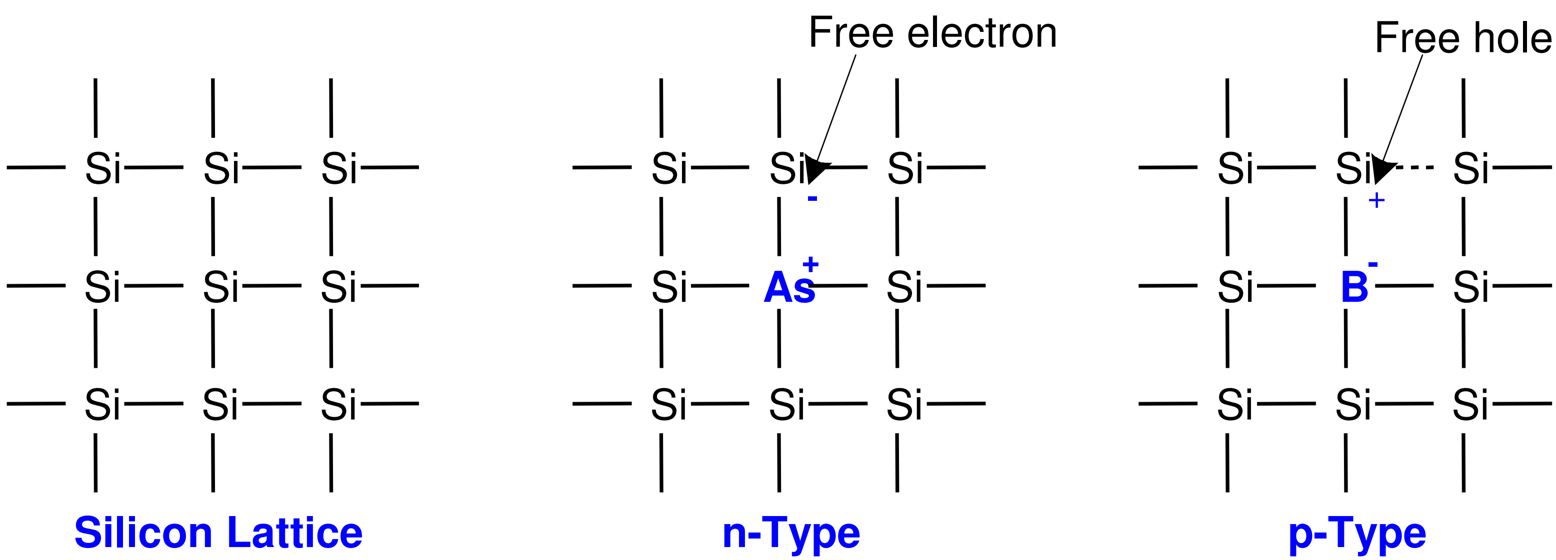
Open switch
when $V_G = V_{DD}$



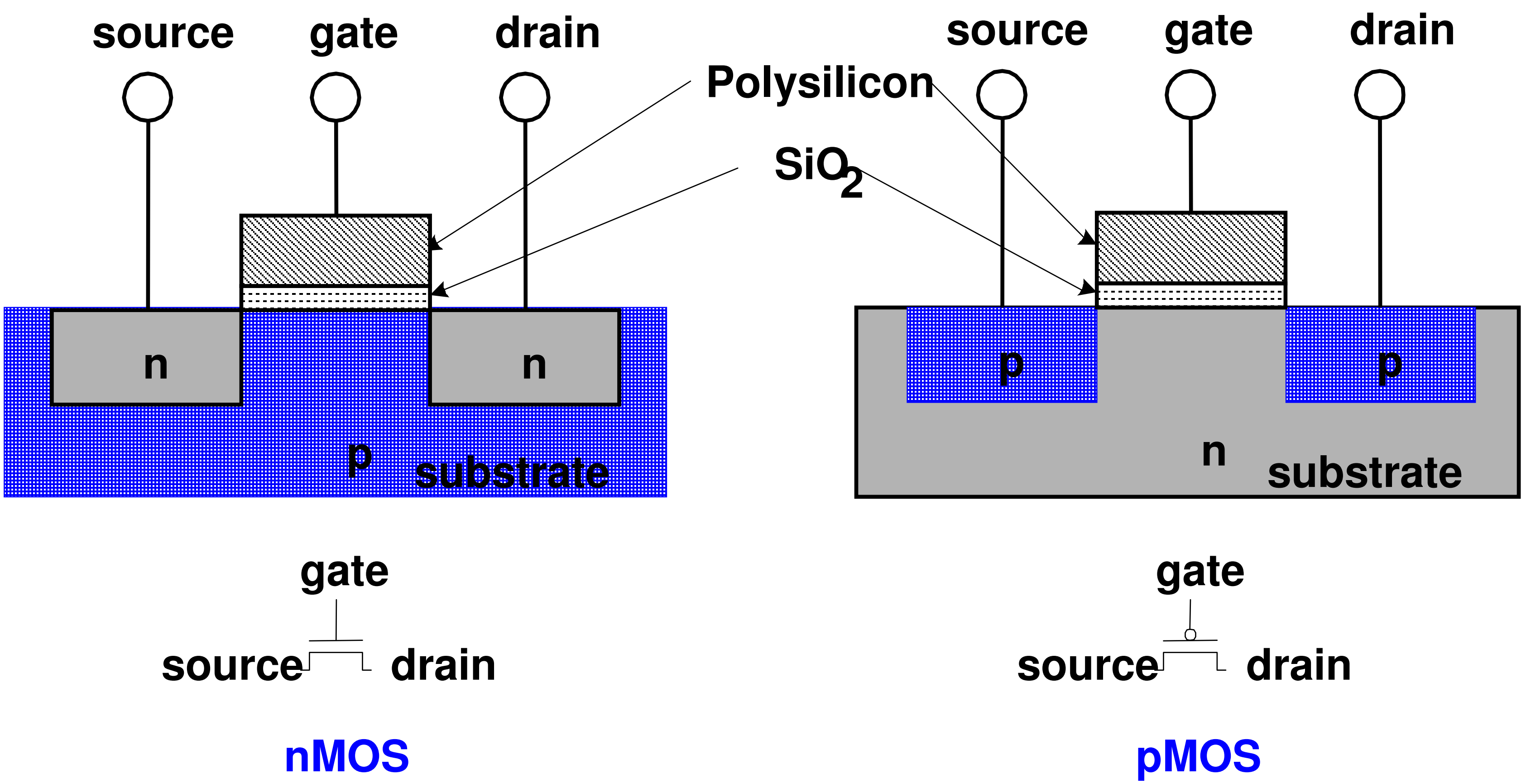
Closed switch
when $V_G = 0$ V

Transistores

- Transistores são construídos com silício, um semicondutor
- Silício não é condutor (não tem cargas livres)
- Quando dopado torna-se condutor (tem cargas livres)
  - n-type
  - p-type

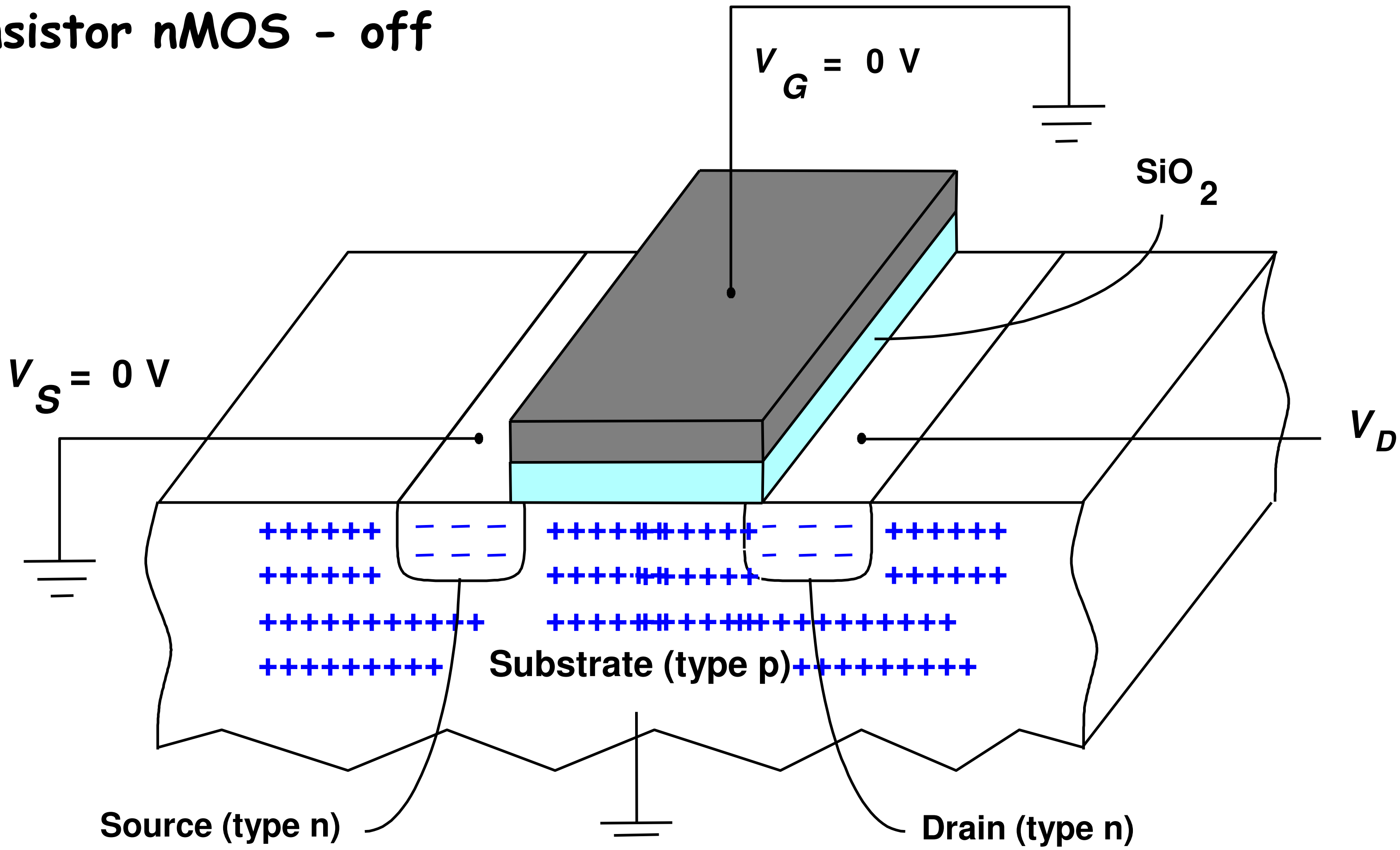


Transistor MOS



CMOS: Fabricação e Comportamento

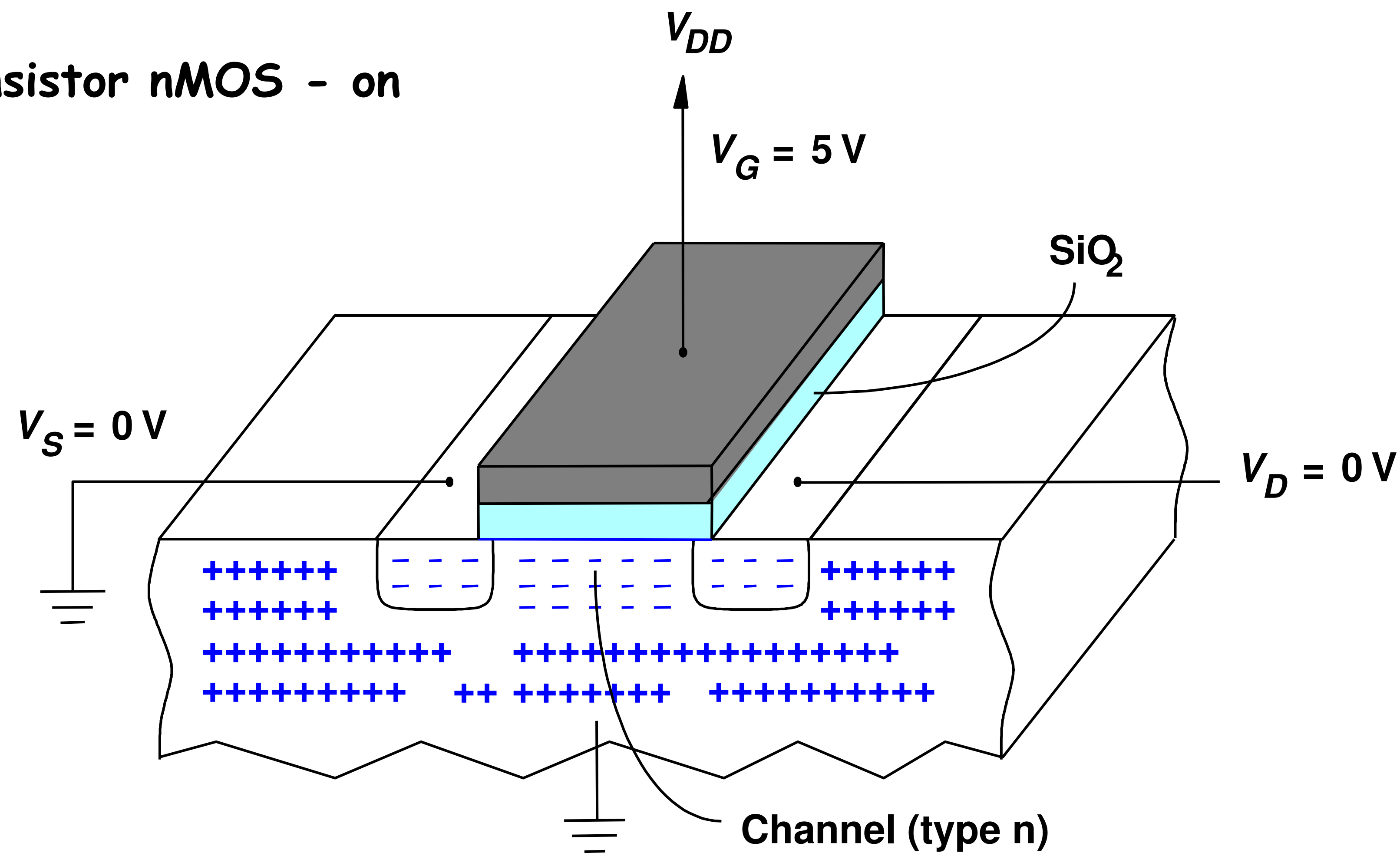
Transistor nMOS - off



When $V_{GS} = 0$ V, the transistor is off

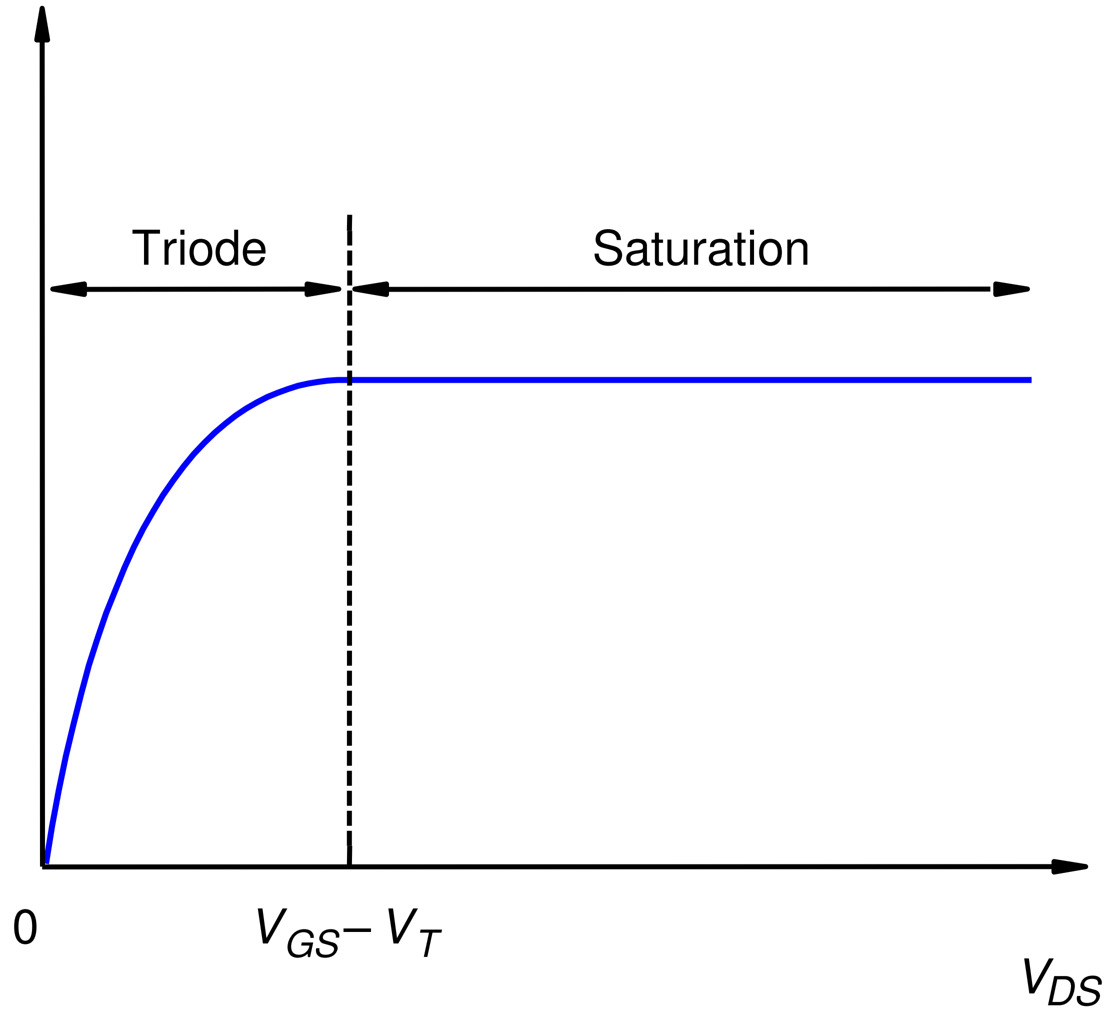
CMOS: Fabricação e Comportamento

Transistor nMOS - on



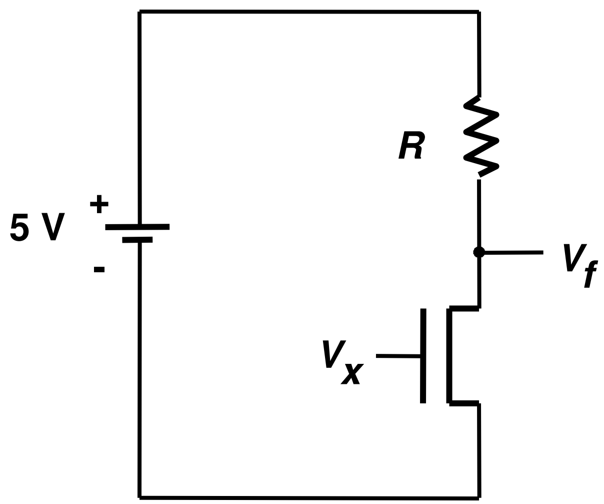
When V_{GS} = 5 V, the transistor is on

Transistor nMOS

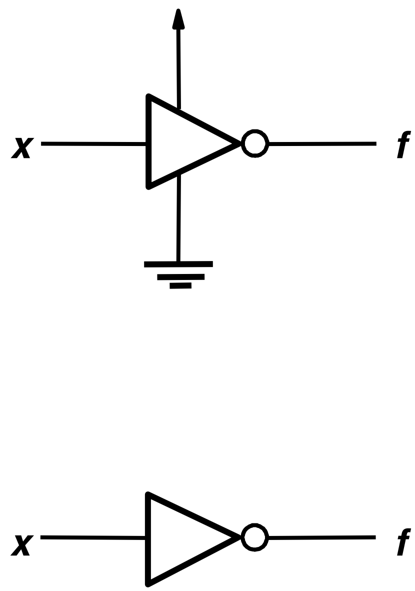


Current-voltage relationship in the NMOS transistor

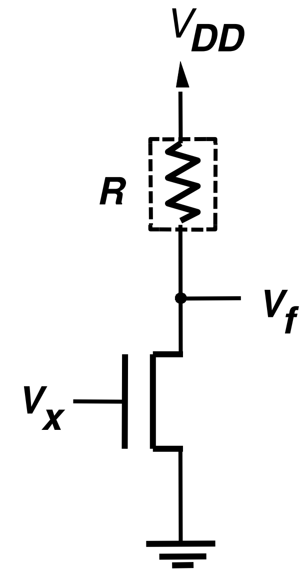
Portas Lógicas com nMOS



Circuit diagram



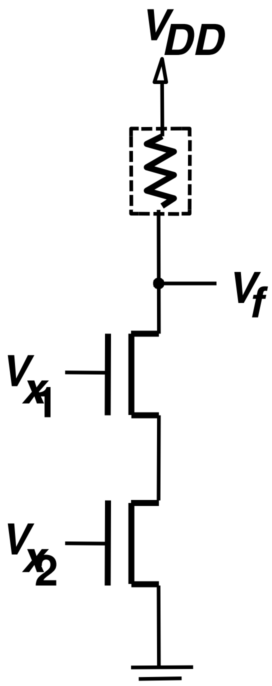
Graphical symbols



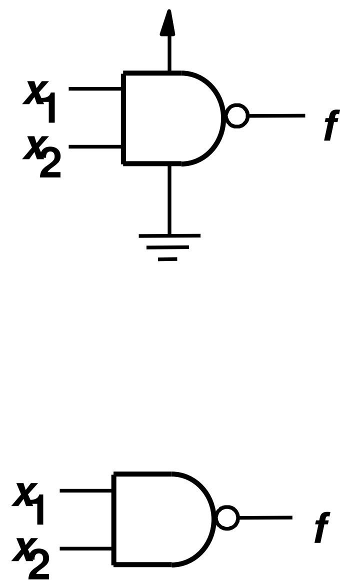
Simplified circuit diagram

A NOT gate built using nMOS technology

Portas Lógicas com nMOS (NAND)



Circuito

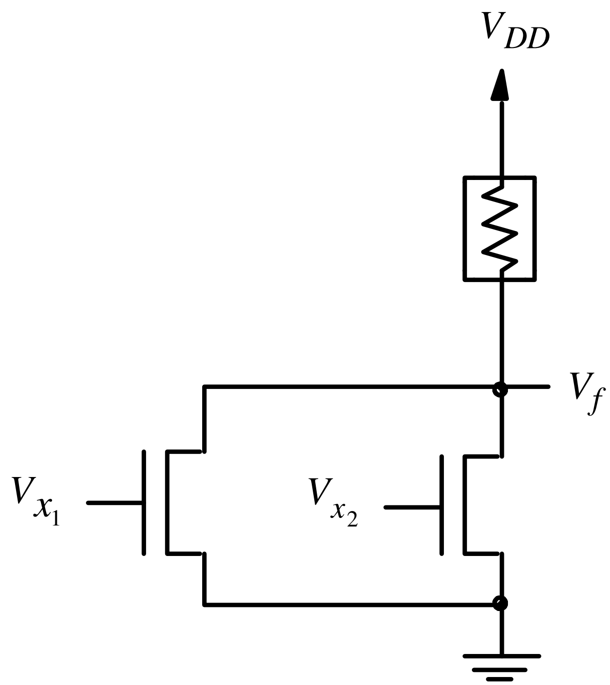


Símbolo grafico

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

Tabela Verdade

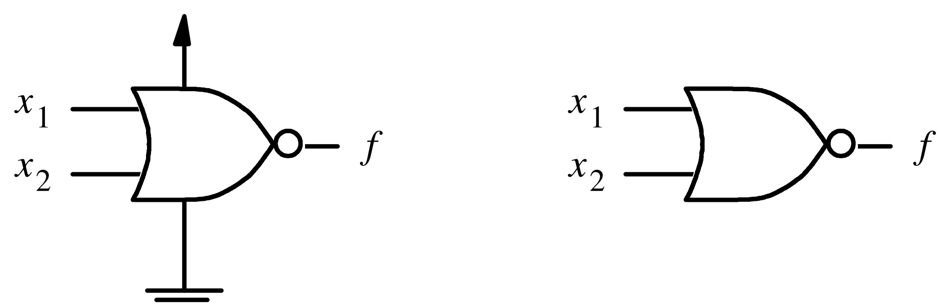
Portas Lógicas com nMOS (NOR)



(a) Circuit

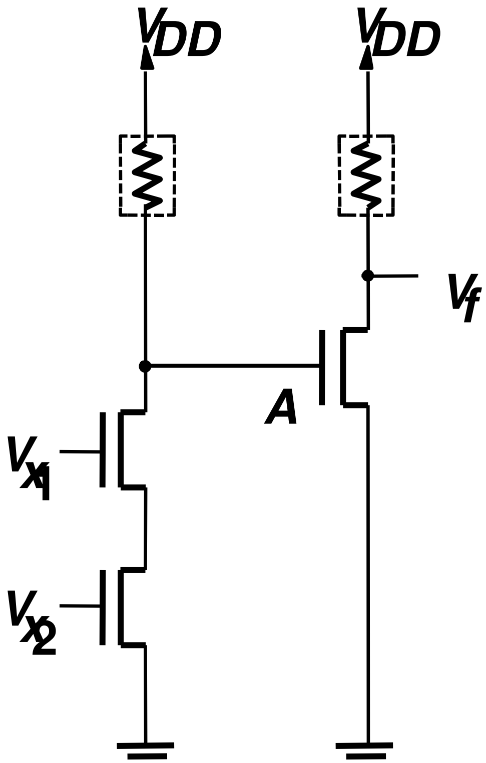
x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

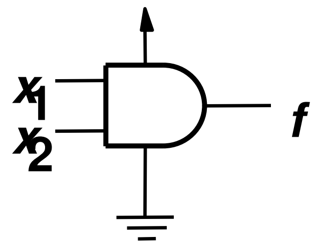
(b) Truth table

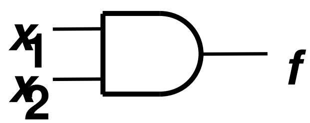


(c) Graphical symbols

Portas Lógicas com nMOS (AND)

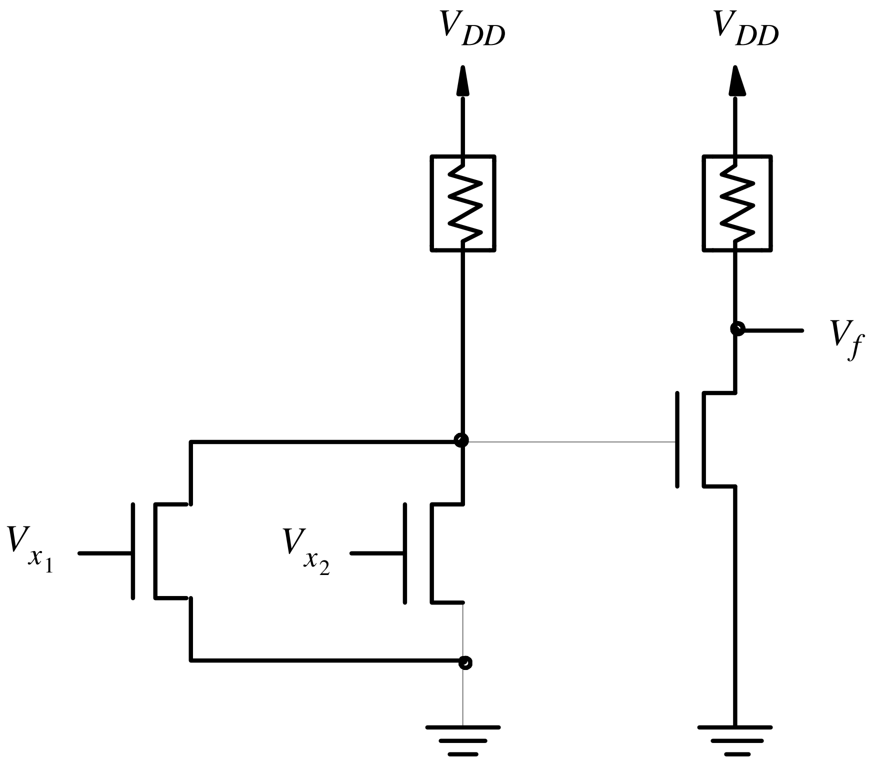






x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

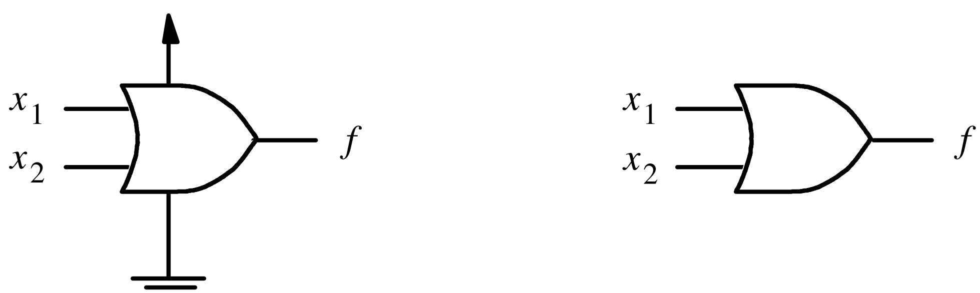
Portas Lógicas com nMOS (OR)



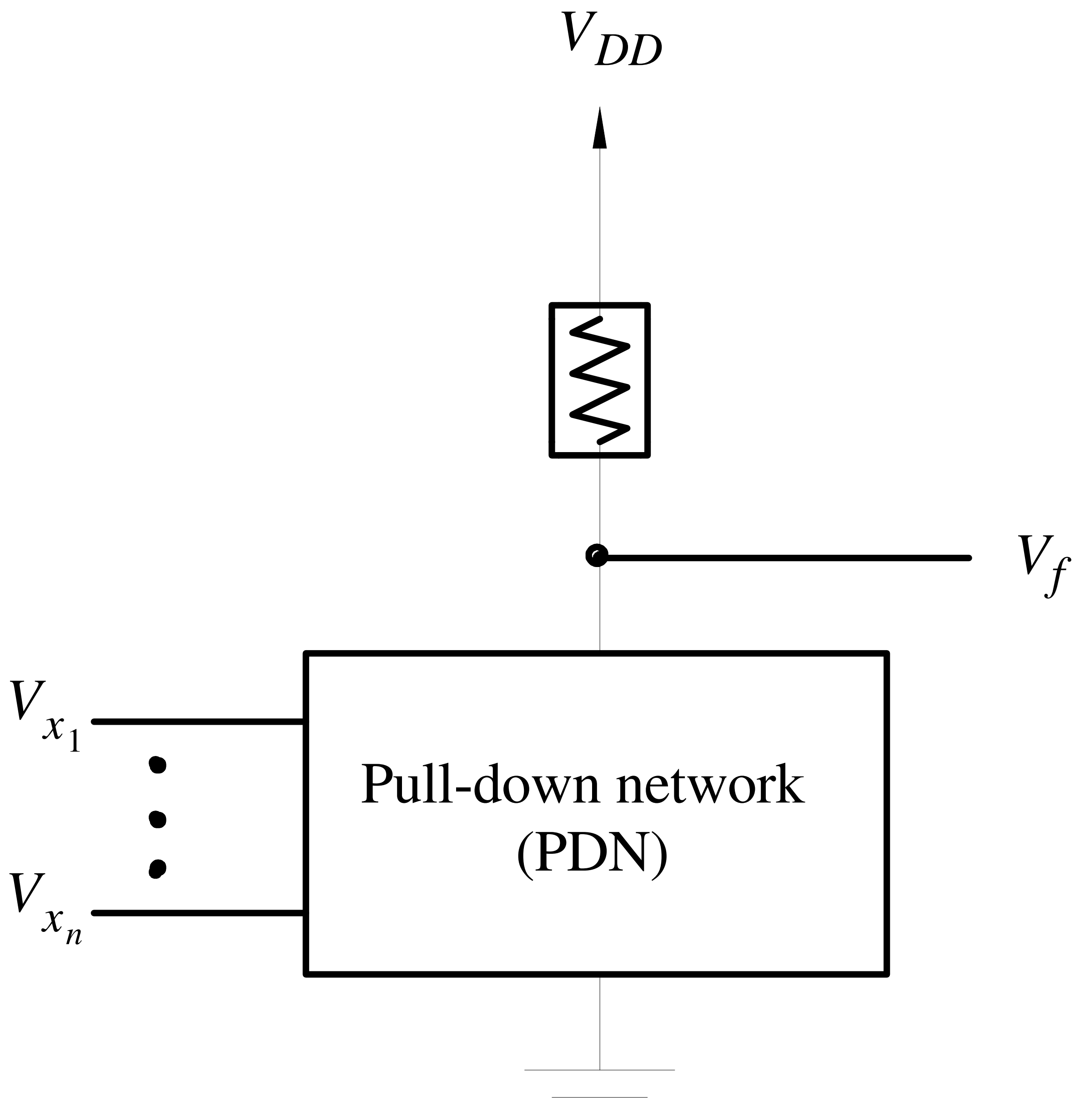
(a) Circuit

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table

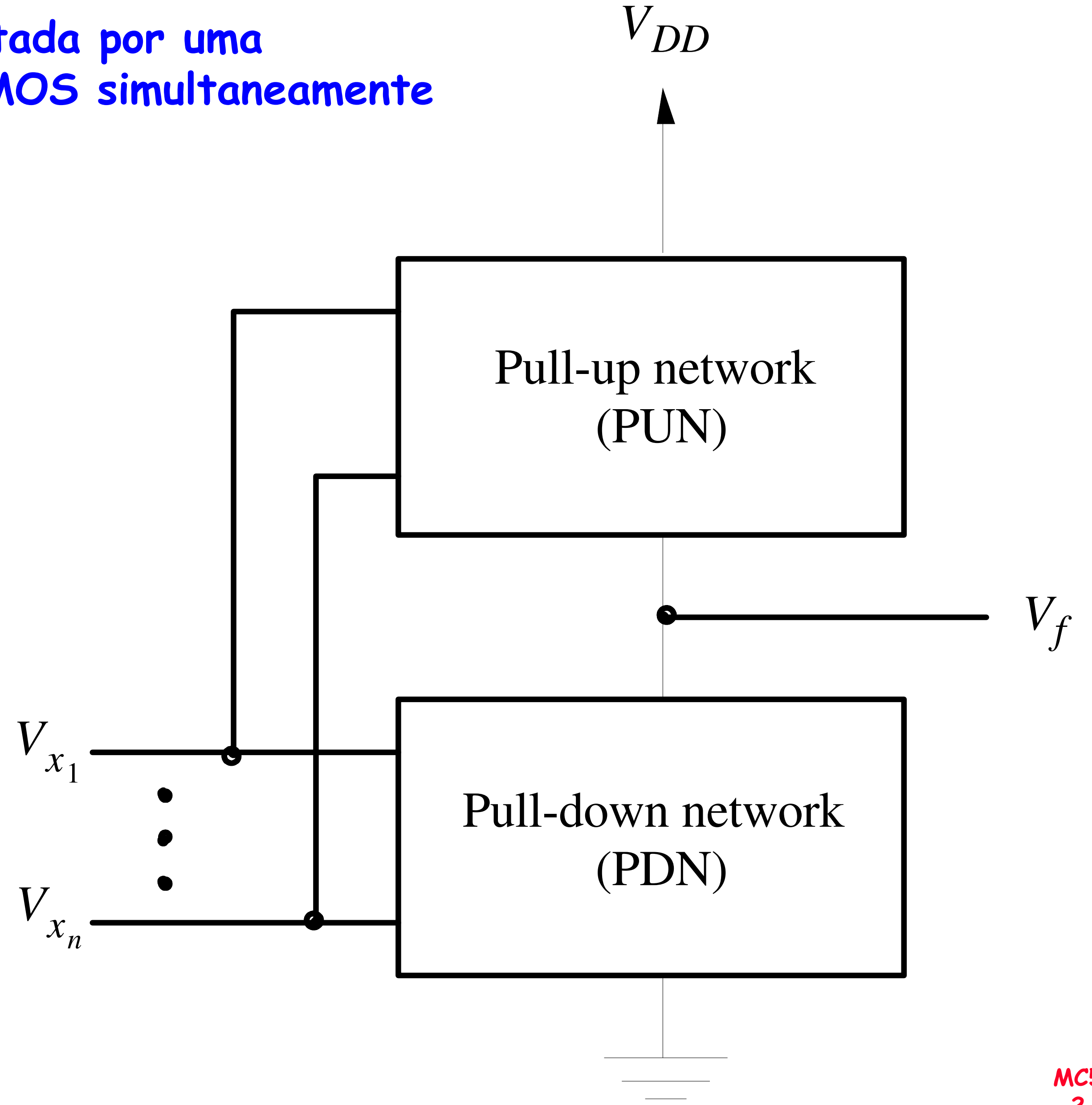


Estrutura de um circuito nMOS

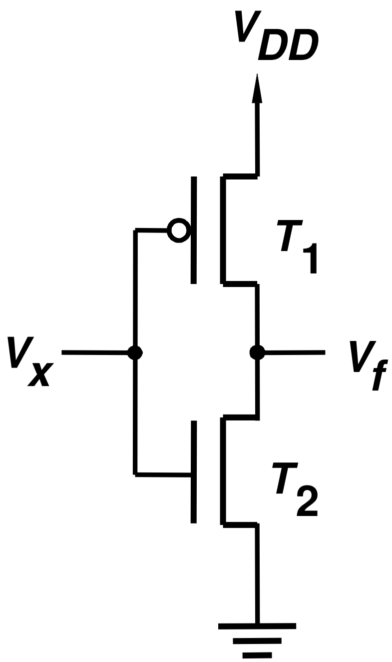


Estrutura de um Circuito CMOS (nMOS + pMOS)

A função é implementada por uma rede nMOS e uma pMOS simultaneamente



NOT CMOS

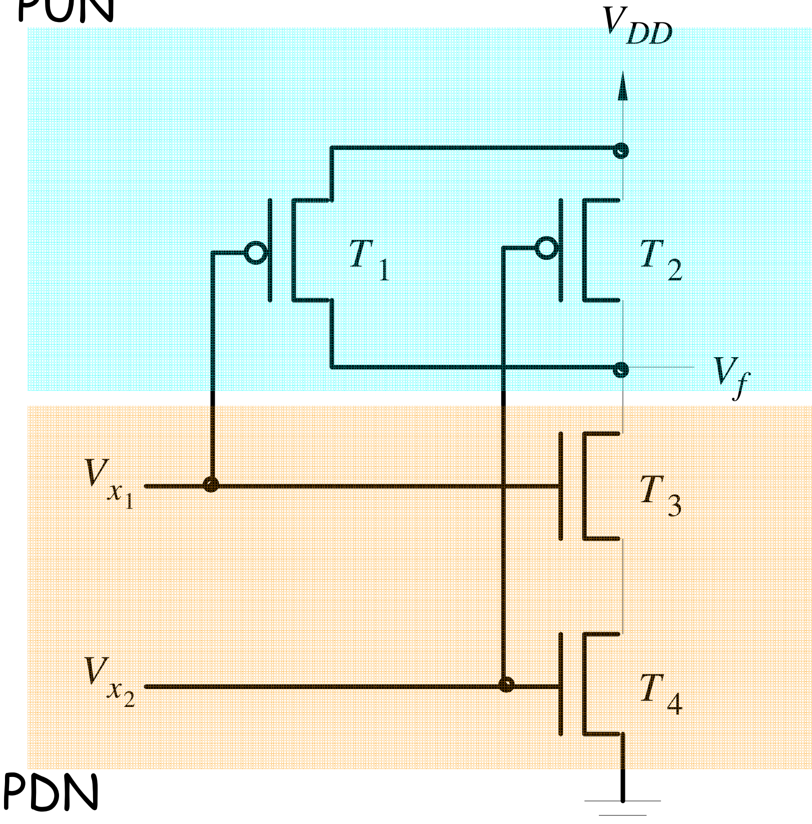


x	T_1	T_2	f
0	on	off	1
1	off	on	0

NAND CMOS

$f = \overline{x_1} + \overline{x_2}$

PUN



PDN

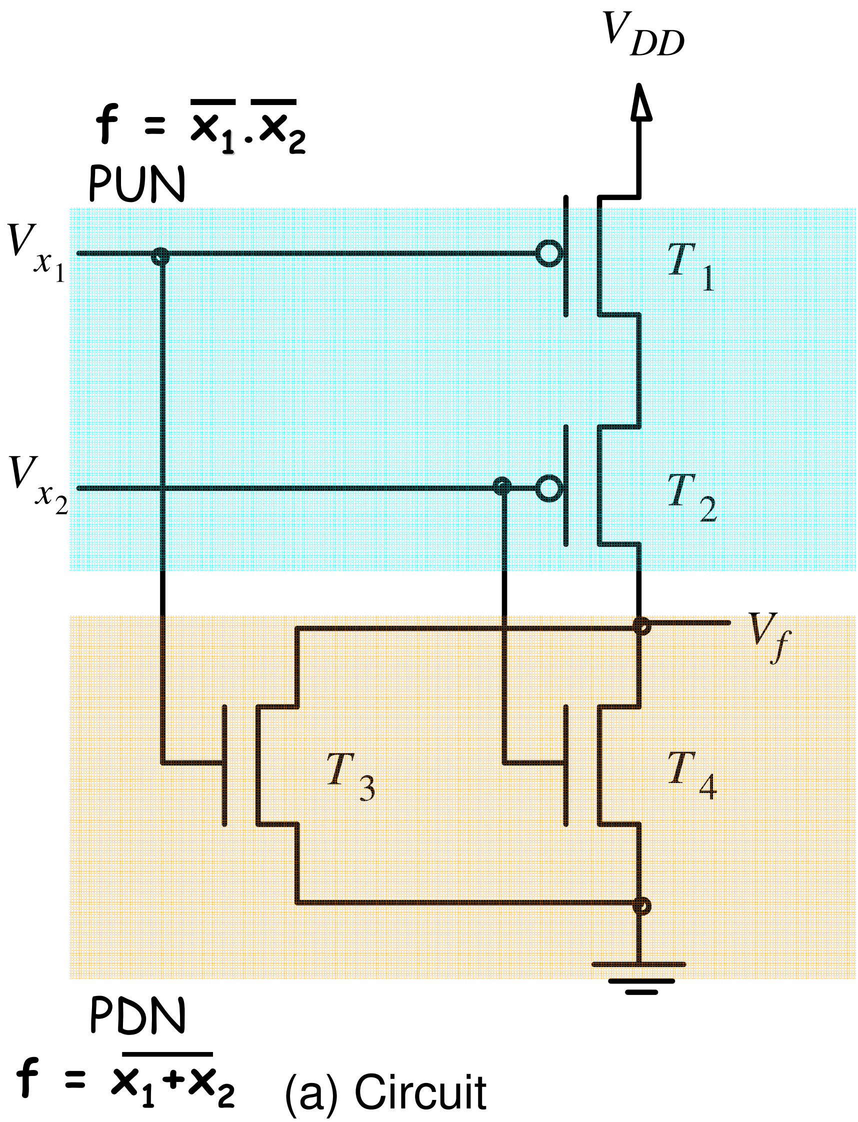
$f = \overline{x_1 . x_2}$

(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

NOR CMOS

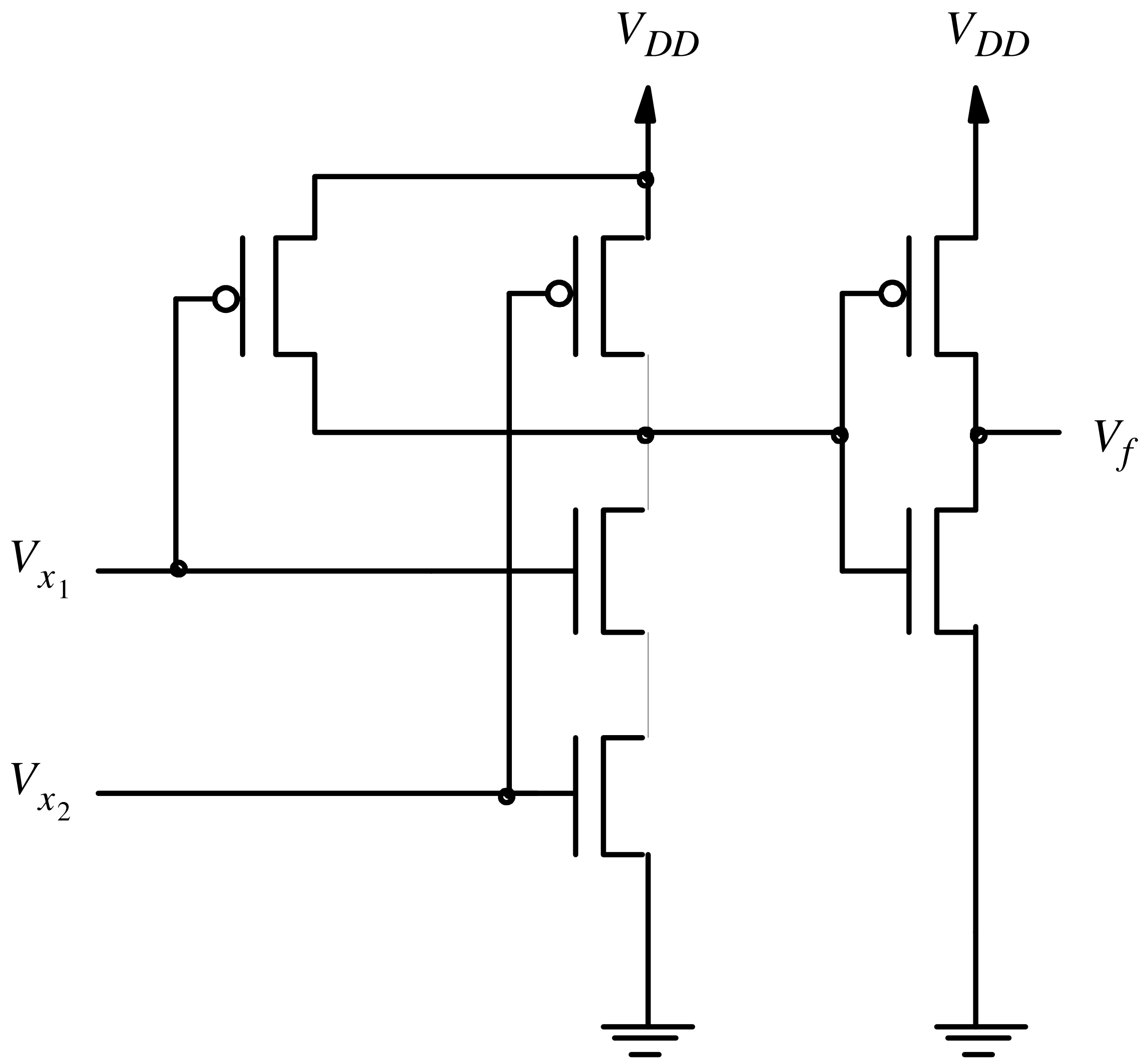


(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

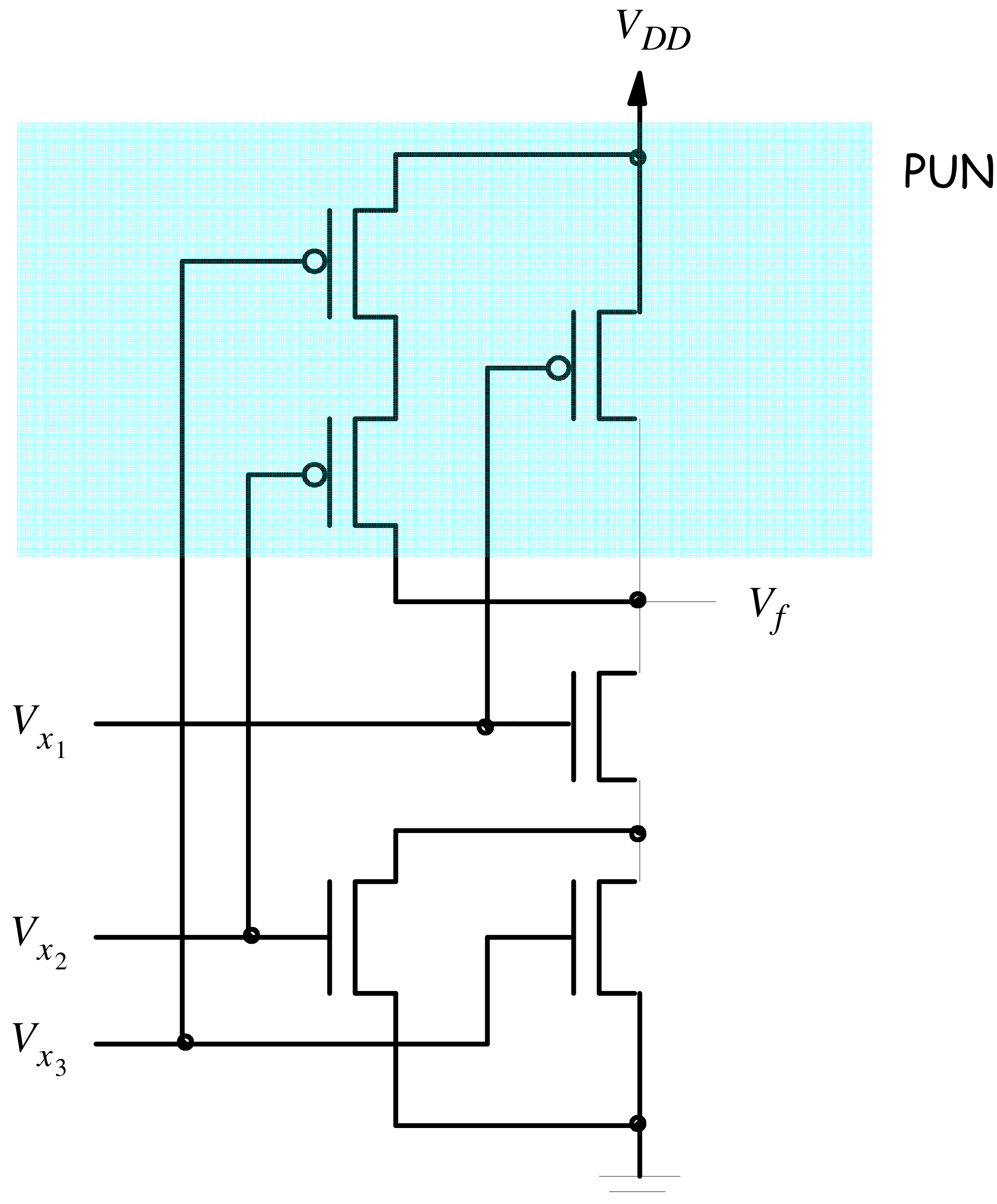
(b) Truth table and transistor states

AND CMOS



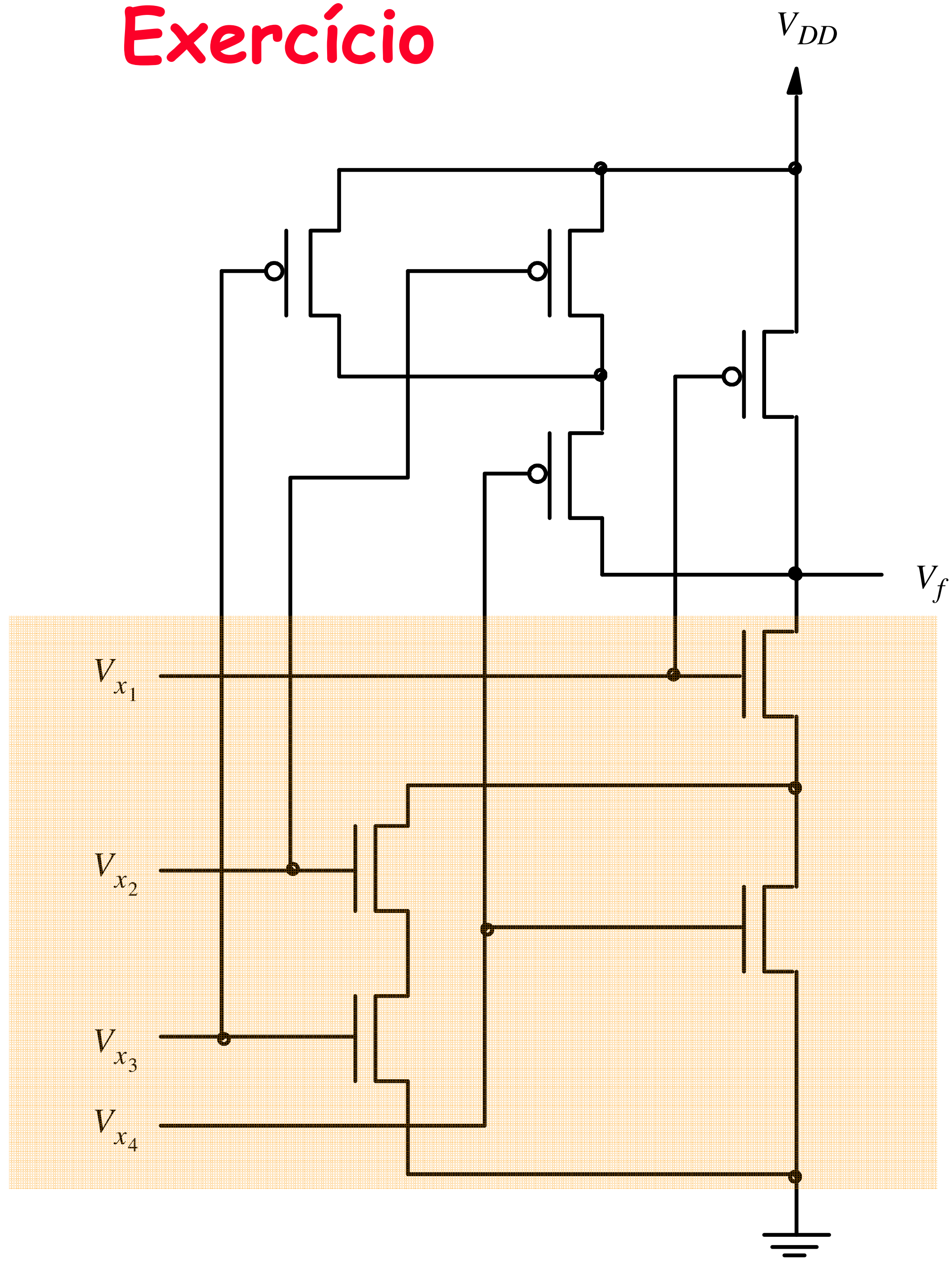
Exemplo: Circuito Complexo

$f = \overline{x_1} + \overline{x_2}\ \overline{x_3}$



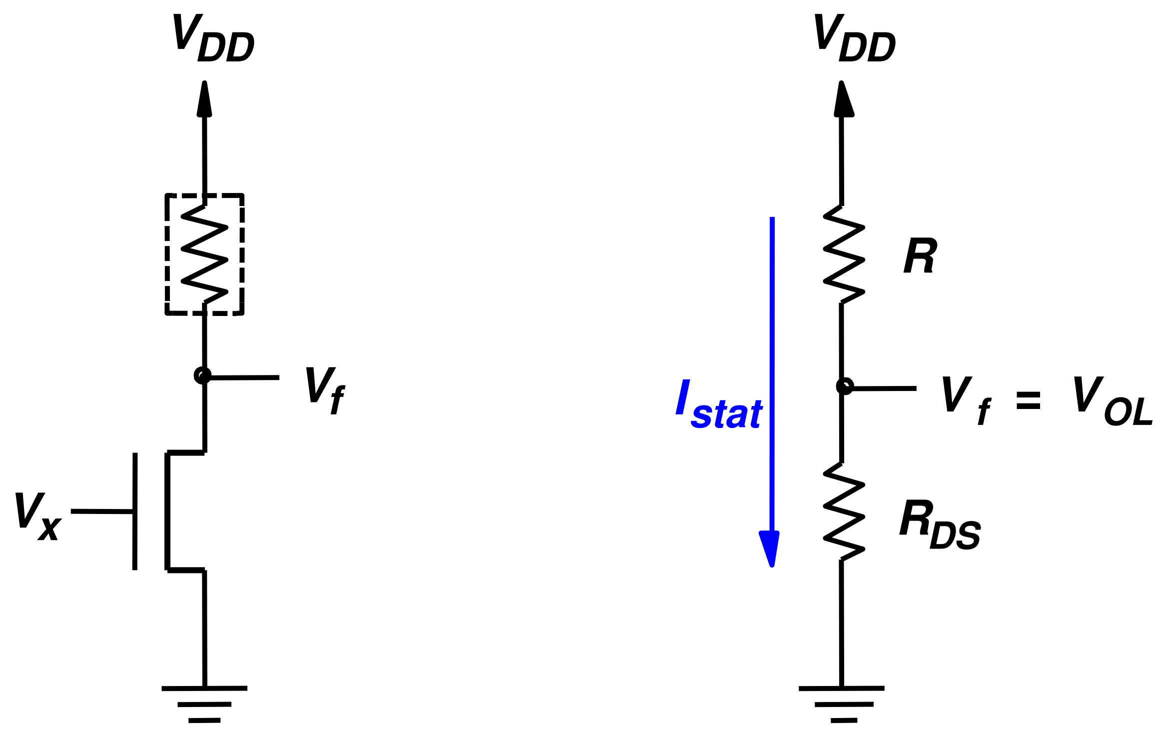
Exercício

Qual a função implementada por:



$\overline{f} = x_1\ (x_2x_3 + x_4)$

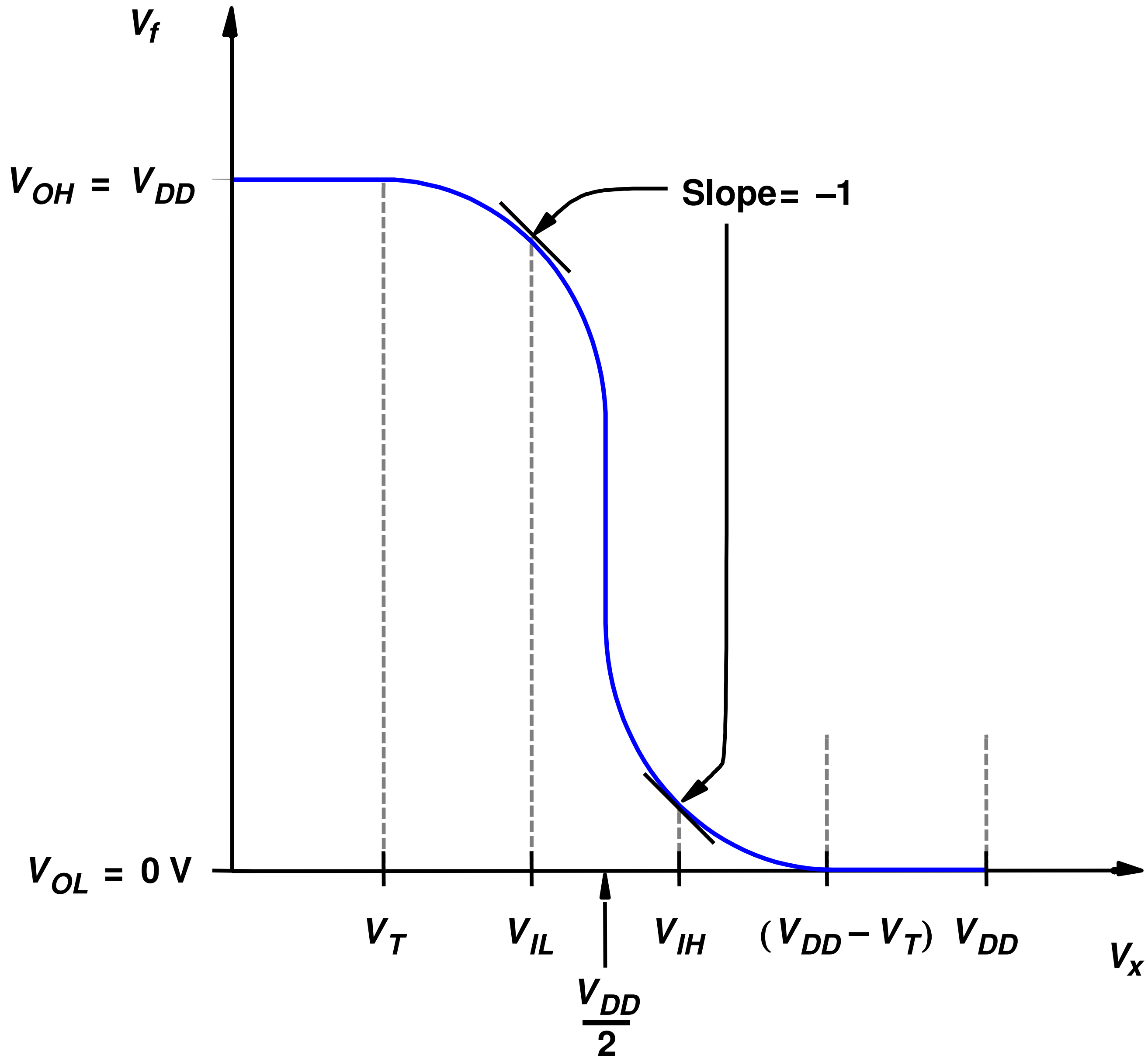
Tensões em um Not nMOS



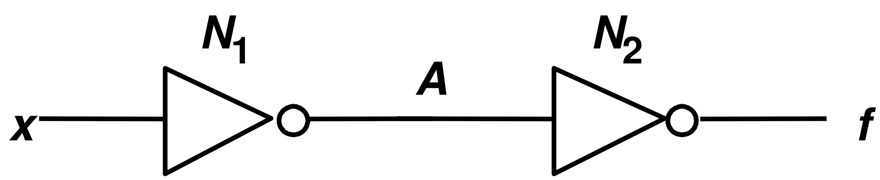
(a) NMOS NOT gate

(b) $V_x = 5$ V

Transferência de Voltagem
Not CMOS



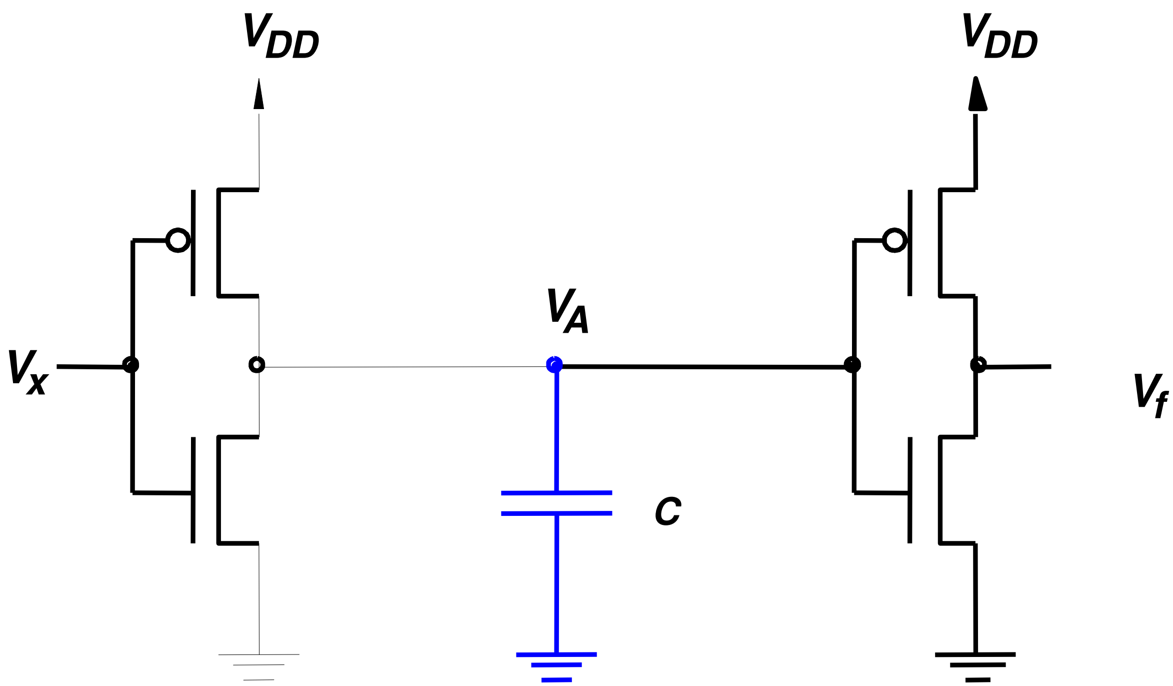
Margem de Ruído e Capacitância



NOT gate driving another NOT gate

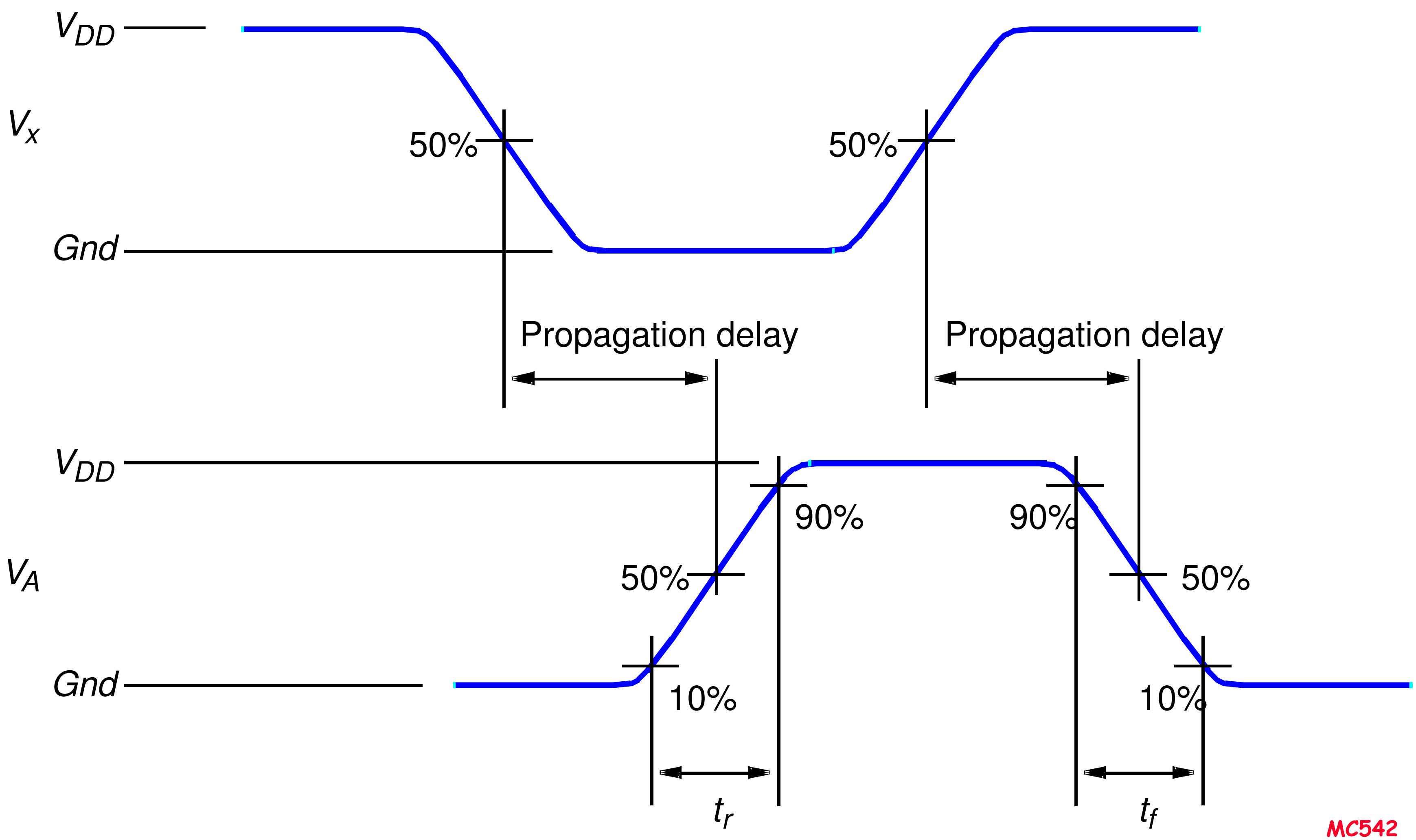
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

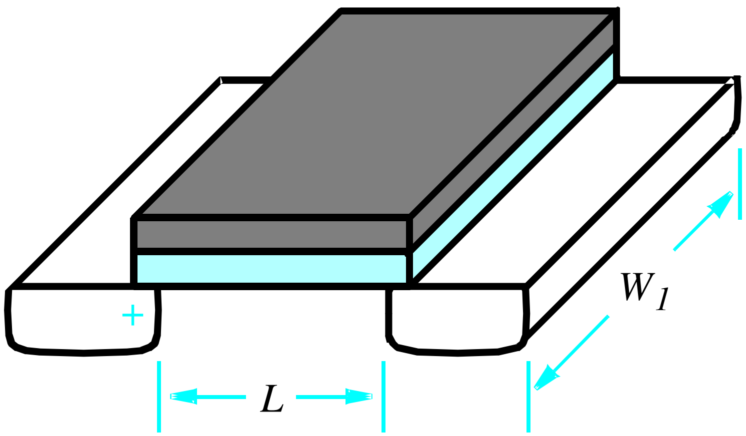


The capacitive load at node A

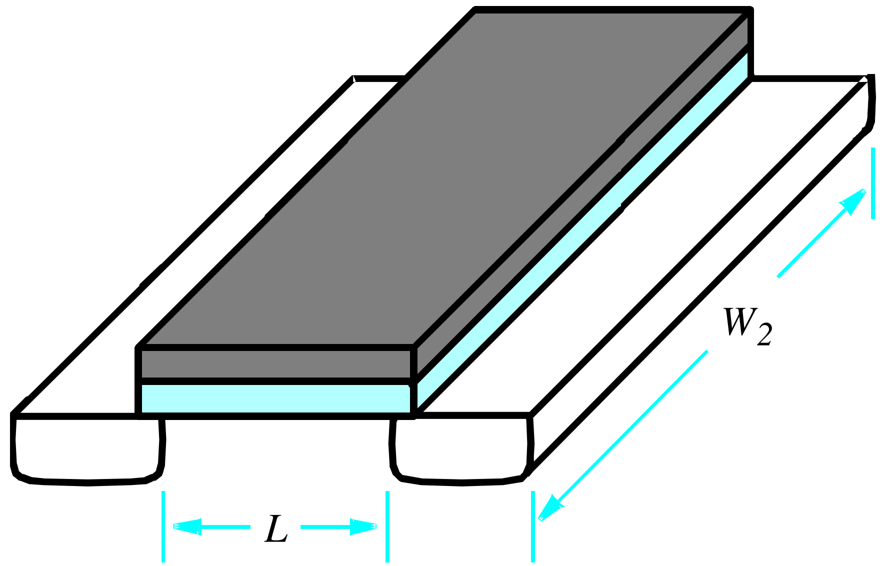
Margem de Ruído e Capacitância



Transistor MOS

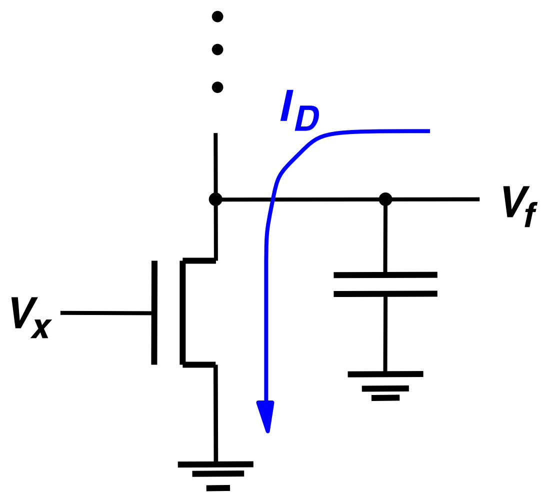


(a) Small transistor

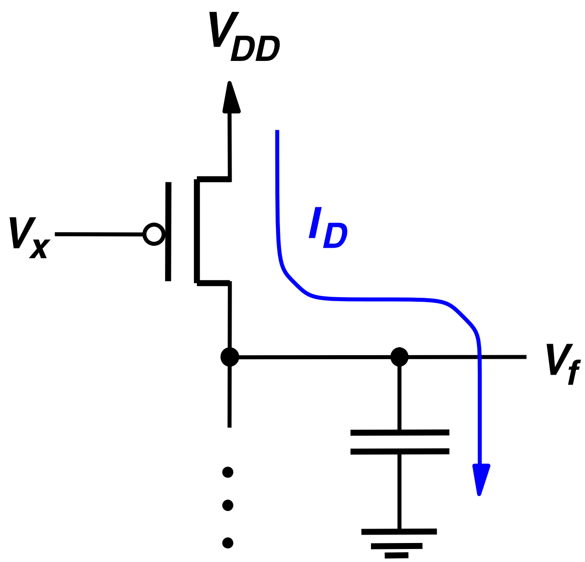


(b) Larger transistor

Consumo de Potência

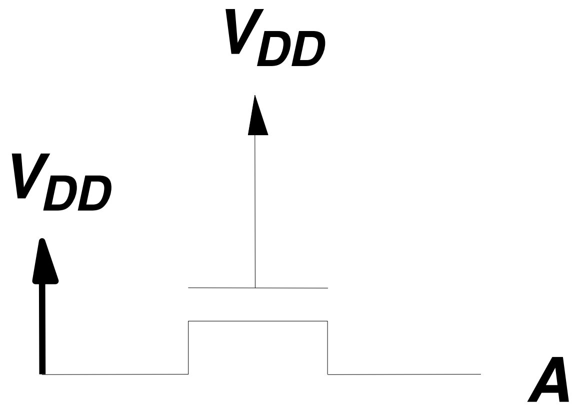


Current flow when input V_x changes from 0 V to 5 V

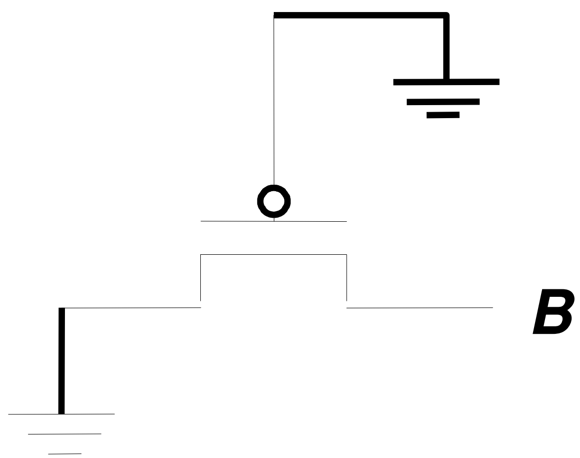


Current flow when input V_x changes from 5 V to 0 V

Passagem de 1s e 0s em MOS

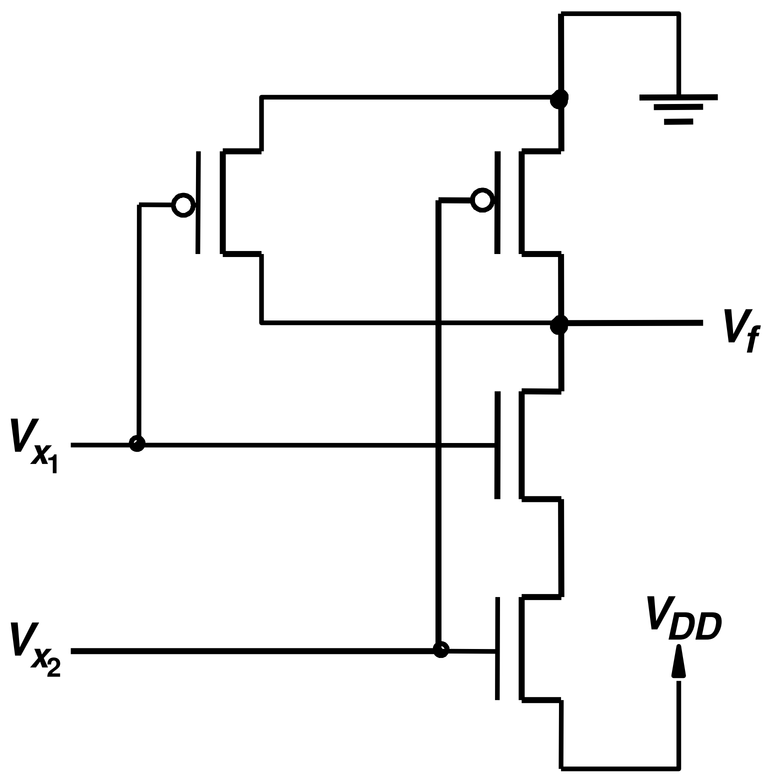


transistor nMOS



transistor pMOS

Implementação "pobre" de um AND CMOS



AND gate circuit

Logic value		Voltage	Logic value
x_1	x_2	V_f	f
0	0	1.5 V	0
0	1	1.5 V	0
1	0	1.5 V	0
1	1	3.5 V	1

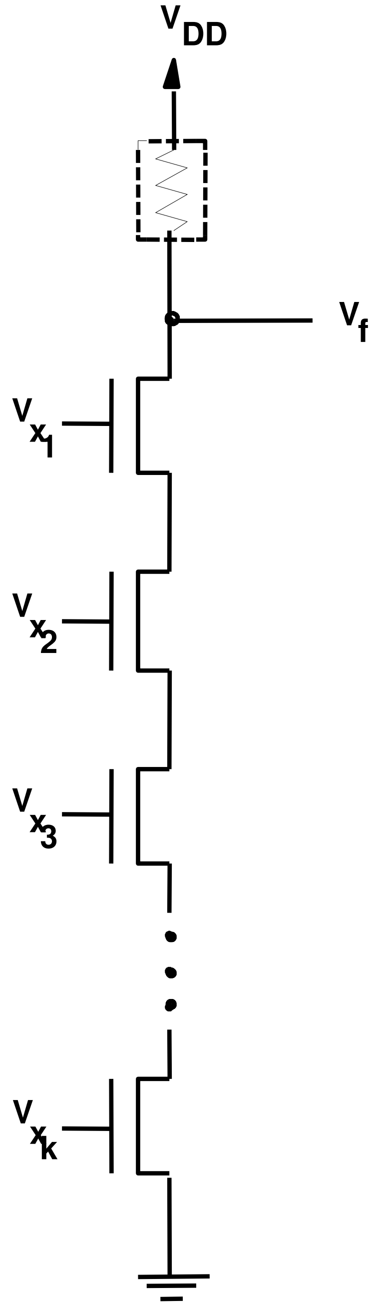
Truth table and voltage levels

Fan-IN

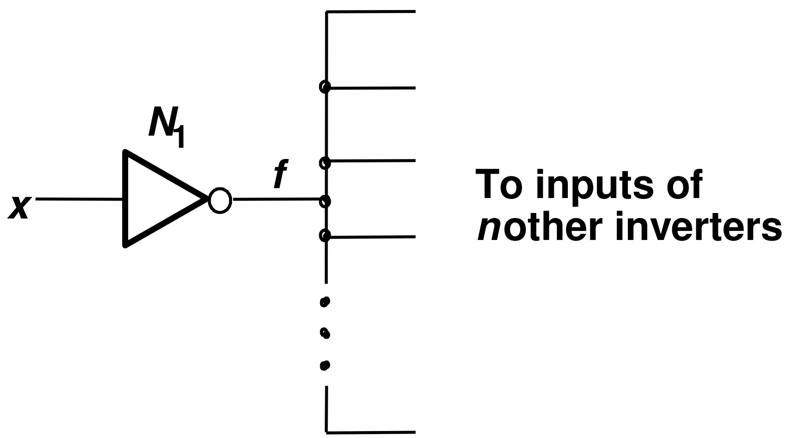
$$R = r_1 + r_2 + \dots + r_k$$

↑ Atraso

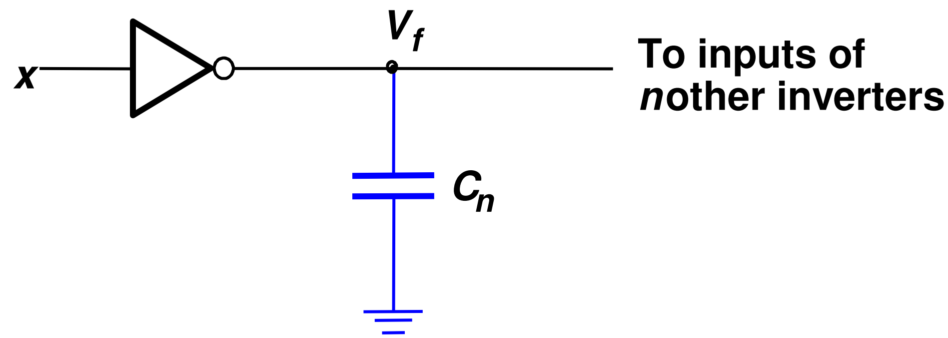
↑ V_f → "0"



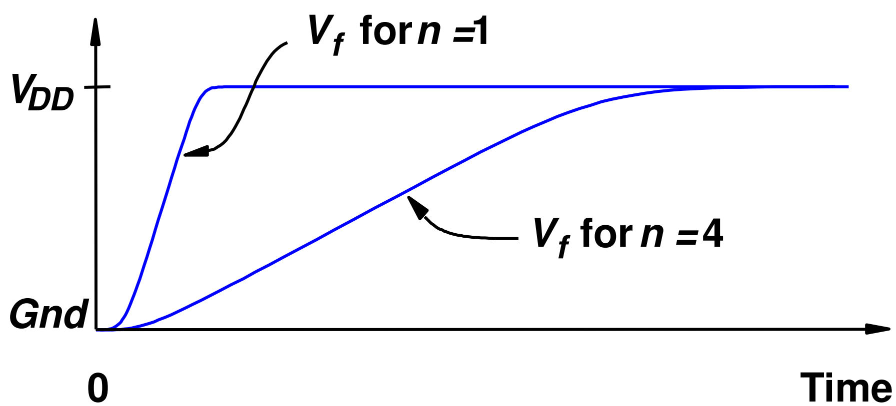
Fan-Out



inverter that drives n other inverters

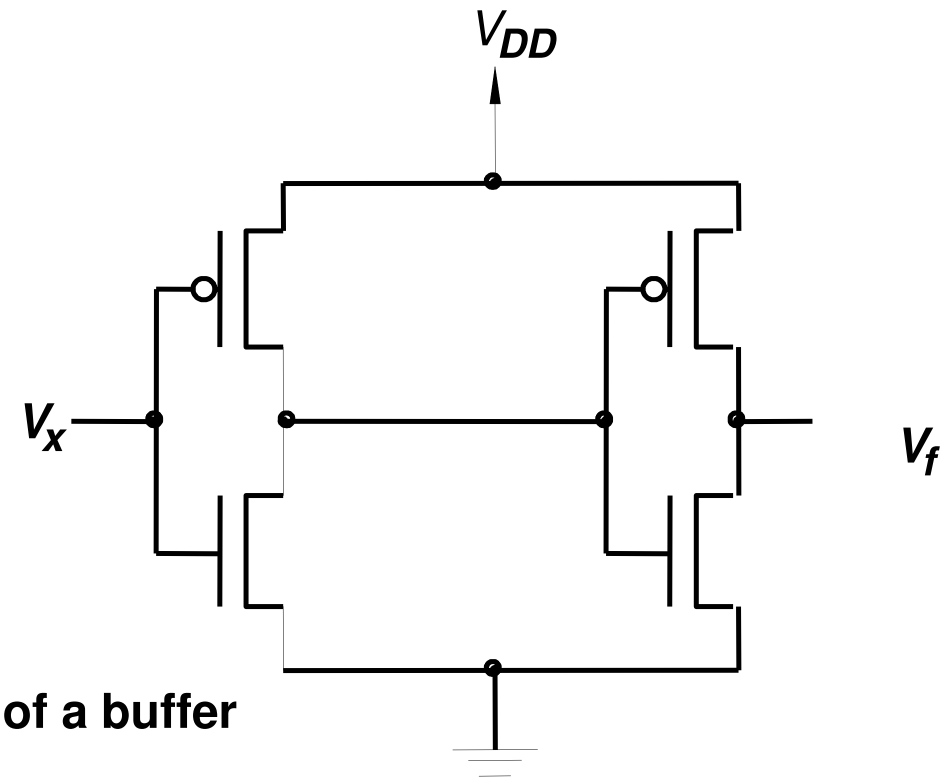


Equivalent circuit for timing purposes

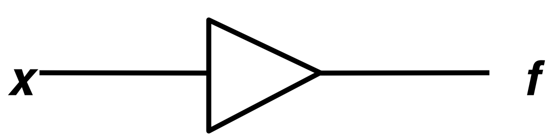


Propagation times for different values of n

Buffer

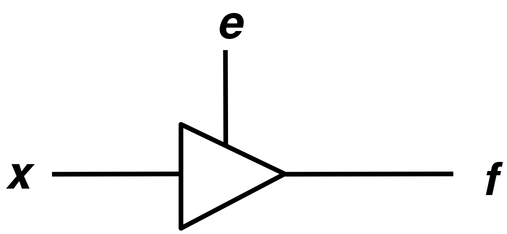


Implementation of a buffer

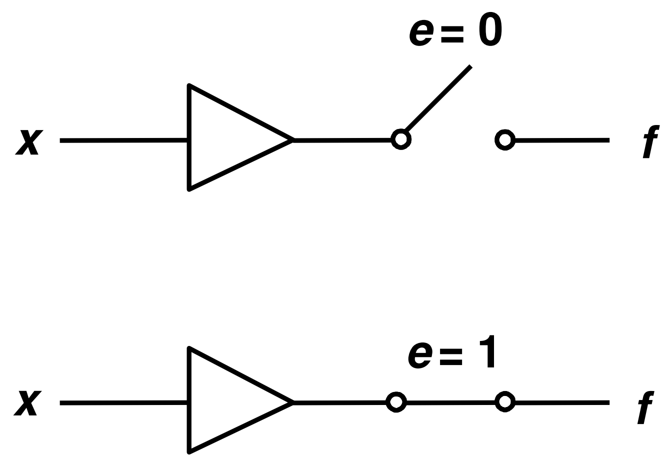


Graphical symbol

Tri-state



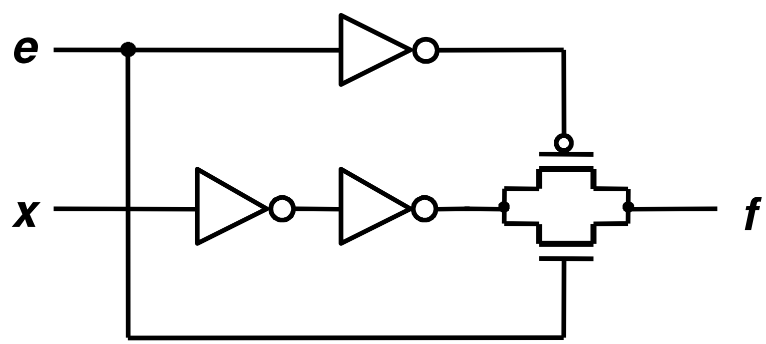
tri-state buffer



Equivalent circuit

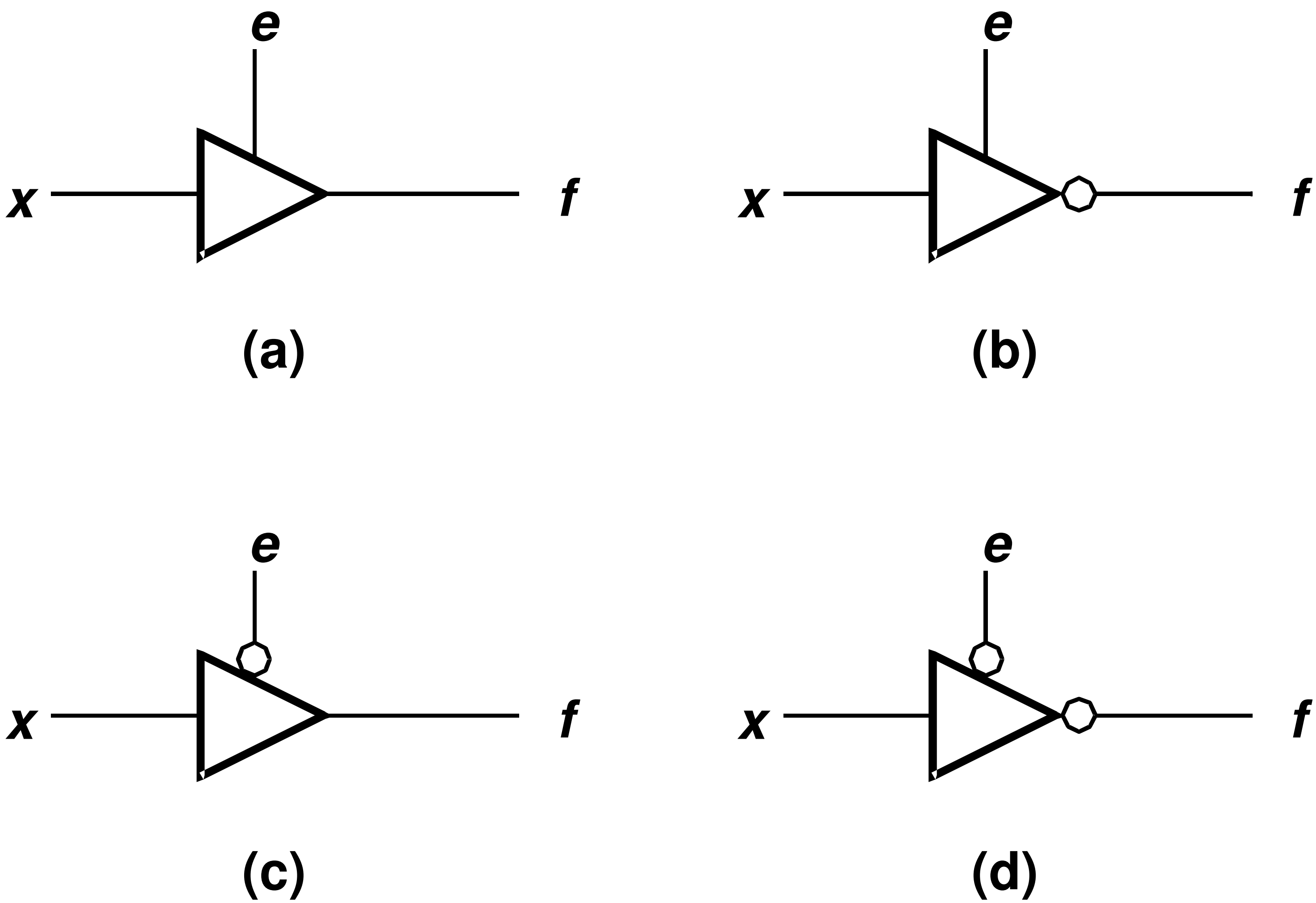
e	*x*	*f*
0	0	Z
0	1	Z
1	0	0
1	1	1

Truth table

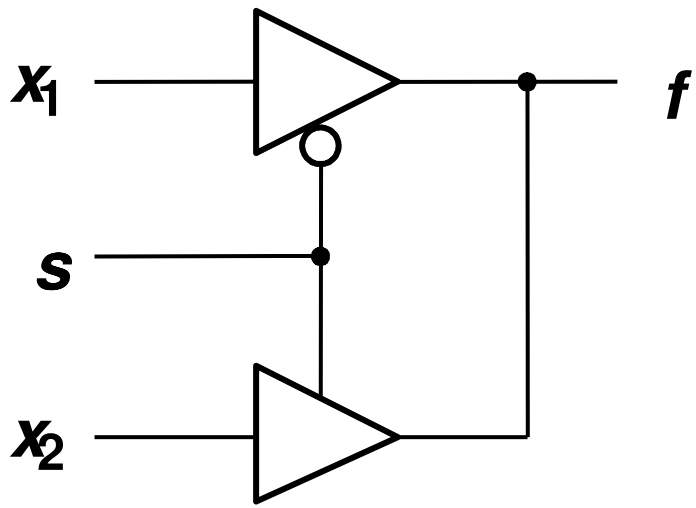


Implementation

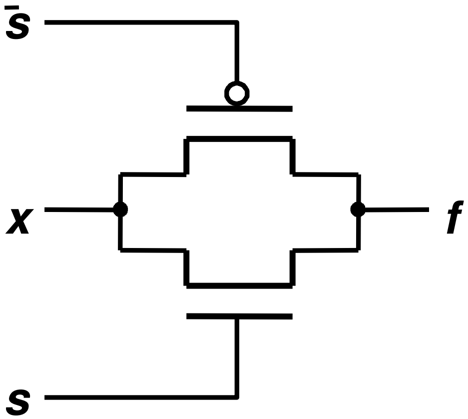
Tri-state



Uso de tri-state



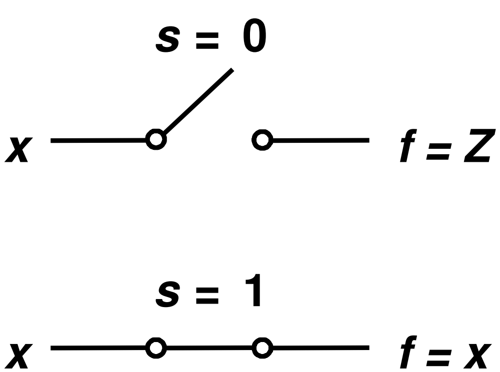
Transmission Gates



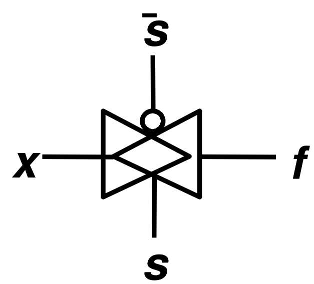
Circuit

s	f
0	Z
1	*x*

Truth table



Equivalent circuit

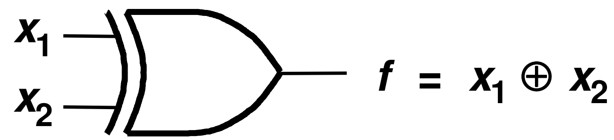


Graphical symbol

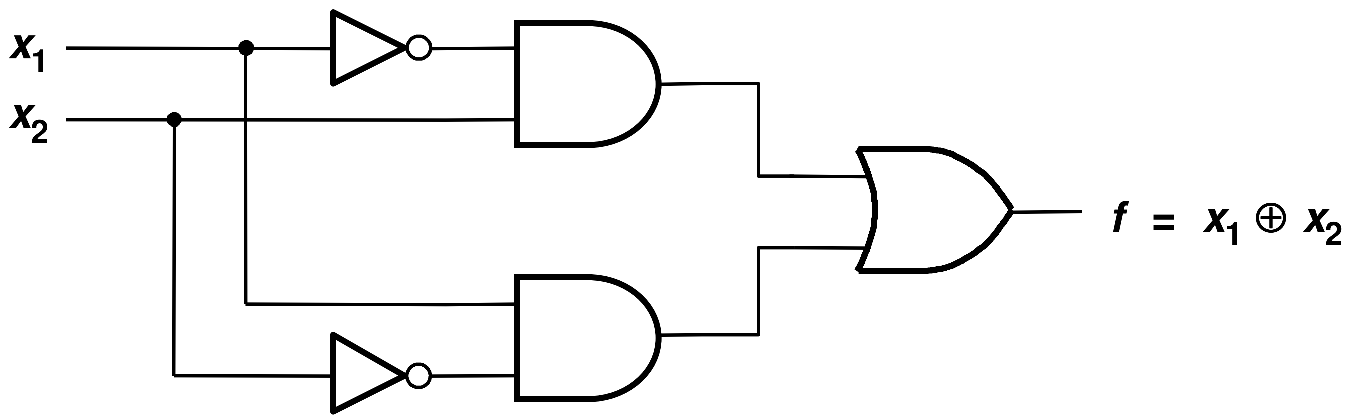
XOR

x_1	x_2	$f = x_1 \oplus x_2$
0	0	0
0	1	1
1	0	1
1	1	0

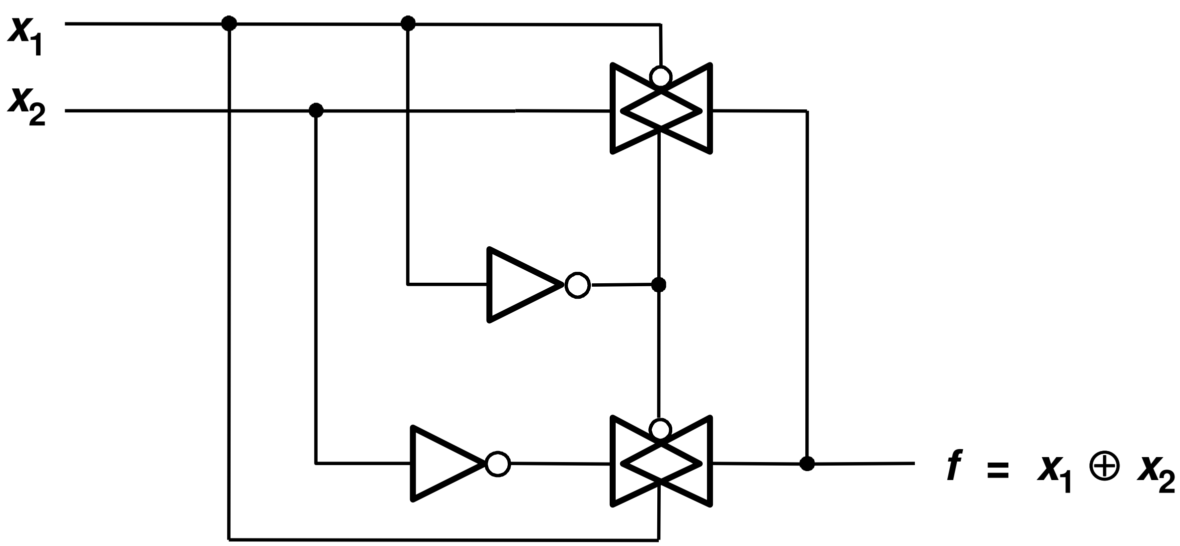
Truth table



Graphical symbol



XOR - Transmission Gate



Mux - Transmission Gate