# MC542

## Organização de Computadores
## Teoria e Prática

2007 - 2011

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# MC542

## Circuitos Lógicos

### Portas Lógicas, Tecnologia

"DDCA" - (Capítulo 1)
"FDL" - (Capítulo 3)



## Portas Lógicas, Tecnologia
## Sumário





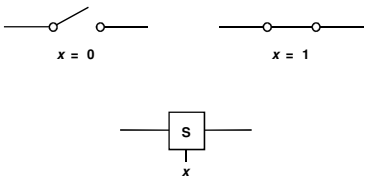
## Portas Lógicas, Tecnologia
## Sumário





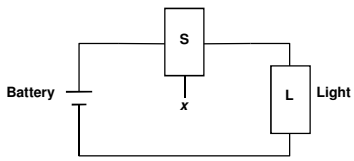
## Variáveis e Funções

Analogia com chaves controladas

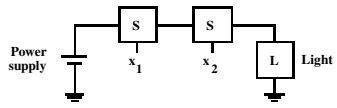




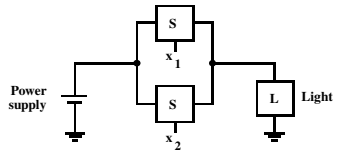

## Variáveis e Funções



## Variáveis e Funções - Funções Simples
AND e OR




Função lógica AND




Função lógica OR

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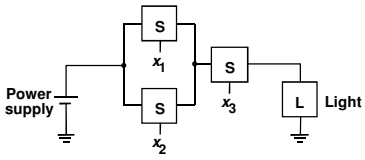
## Variáveis e Funções - Funções Complexas




Arranjo serie/paralelo

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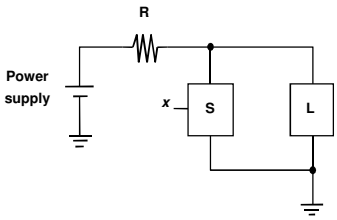
## Variáveis e Funções
NOT




MC542 2.9

## Tabela Verdade

| $x_1$ | $x_2$ | $x_1 \cdot x_2$ | $x_1 + x_2$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 |
| | | AND | OR |

MC542 2.10

## Tabela Verdade

| $x_1$ | $x_2$ | $x_3$ | $x_1 \cdot x_2 \cdot x_3$ | $x_1 + x_2 + x_3$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

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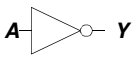
## Portas Lógicas: Uma Entrada (ou Gates)

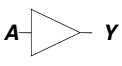
**NOT**




$Y = \overline{A}$

| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

**BUF**




$Y = A$

| A | Y |
|---|---|
| 0 | 0 |
| 1 | 1 |

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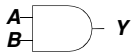
## Portas Lógicas: Duas Entradas

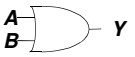
**AND**




$Y = AB$

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**OR**




$Y = A + B$

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



## Portas Lógicas: Duas Entradas

**XOR**


$Y = A \oplus B$

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**NAND**


$Y = \overline{AB}$

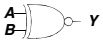
| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**NOR**


$Y = \overline{A + B}$

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**XNOR**



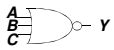

$Y = \overline{A \oplus B}$

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



## Portas Lógicas: Múltiplas Entradas

**NOR3**

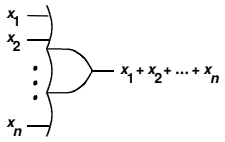



$Y = \overline{A+B+C}$

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

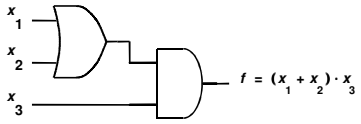
**AND4**


$Y = ABCD$






## Rede Lógica




Rede de portas
Circuito lógico



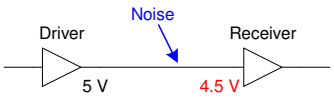
## Níveis Lógicos

- Define as voltagens para representar o 1 e o 0
- Exemplo:
  - 0 : terra ou 0 volts
  - 1 : $V_{DD}$ ou 5 volts
- Qual o valor produzido por uma porta (gate)?
- Se produzir 4.99 volts? Isso é um 0 ou um 1?
- E se 3.2 volts?

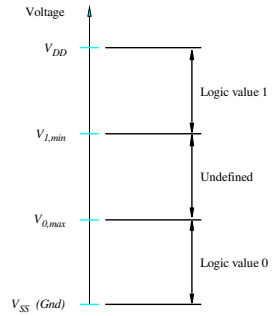


## Níveis Lógicos

- Define-se intervalos de voltagens para representar o 1 e o 0
- Define-se diferentes intervalos para saídas e entradas para permitir tolerância a ruídos
- Ruído é qualquer coisa que degrada o sinal

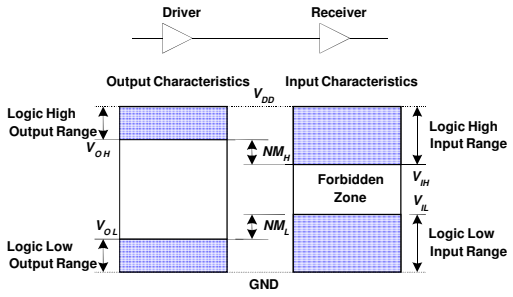


## Níveis Lógicos




MC542 2.19

## Níveis Lógicos: Margem de Ruído




$NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$

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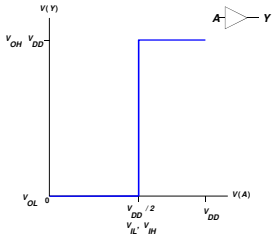
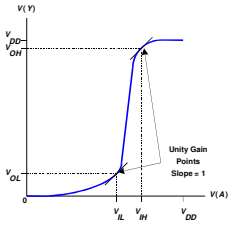
## Característica de Transferência DC

Ideal Buffer:




$NM_H = NM_L = V_{DD}/2$

Real Buffer:




$NM_H, NM_L < V_{DD}/2$

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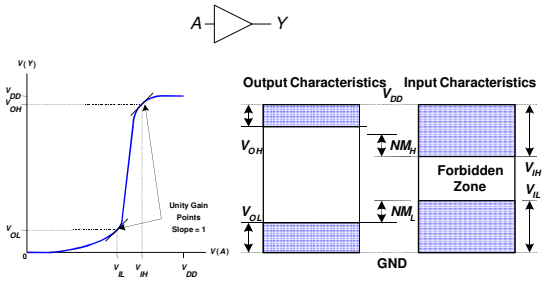
## Característica de Transferência DC

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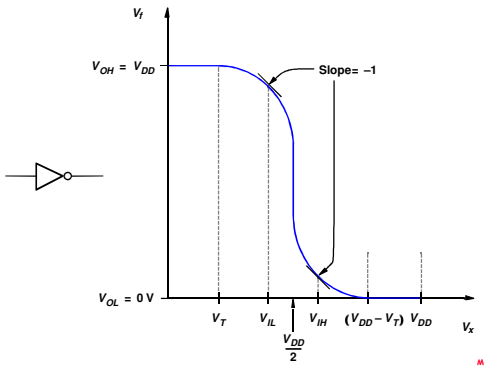
## Característica de Transferência DC



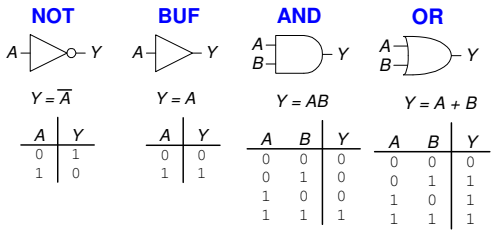

MC542 2.23

## Famílias Lógicas

| Logic Family | $V_{DD}$ | $V_{IL}$ | $V_{IH}$ | $V_{OL}$ | $V_{OH}$ |
|---|---|---|---|---|---|
| TTL | 5 (4.75 - 5.25) | 0.8 | 2.0 | 0.4 | 2.4 |
| CMOS | 5 (4.5 - 6) | 1.35 | 3.15 | 0.33 | 3.84 |
| LVTTL | 3.3 (3 - 3.6) | 0.8 | 2.0 | 0.4 | 2.4 |
| LVCMOS | 3.3 (3 - 3.6) | 0.9 | 1.8 | 0.36 | 2.7 |

MC542 2.24

## Como Construir as Portas Lógicas




**Transistores!**

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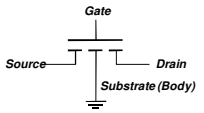
## Transistor como Chave

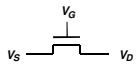

A simple switch controlled by the input *x*

MOSFET: Metal Oxide Semiconductor Field-Effect Transistor




nMOS transistor

MOSFET: nMOS e pMOS




Simplified symbol for an nMOS transistor

nMOS transistor as a switch

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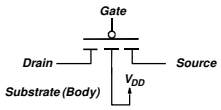
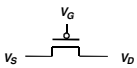
## Transistor como Chave


A switch with the opposite behavior of Figure 3.2




pMOS transistor




Simplified symbol for an pMOS transistor

pMOS transistor as a switch

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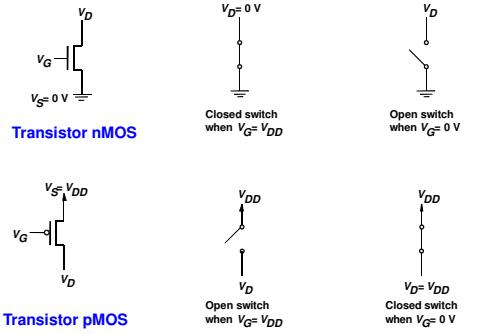
## Comportamento dos Transistores NMOS e PMOS em Circuitos

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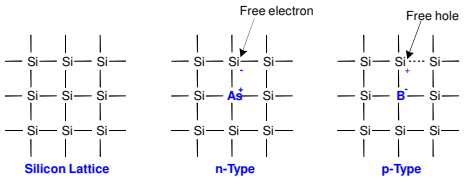
## Transistores

- Transistores são construídos com silício, um semicondutor
- Silício não é condutor (não tem cargas livres)
- Quando dopado torna-se condutor (tem cargas livres)
  - n-type
  - p-type

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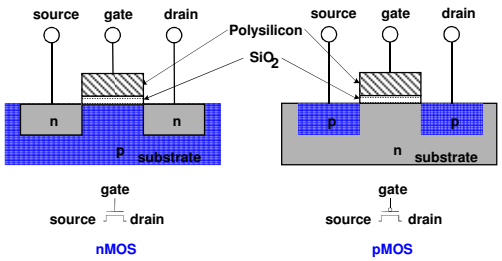
## Transistor MOS

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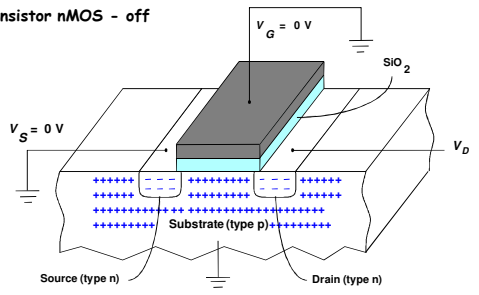
## CMOS: Fabricação e Comportamento

Transistor nMOS - off




When $V_{GS}$ = 0 V, the transistor is off

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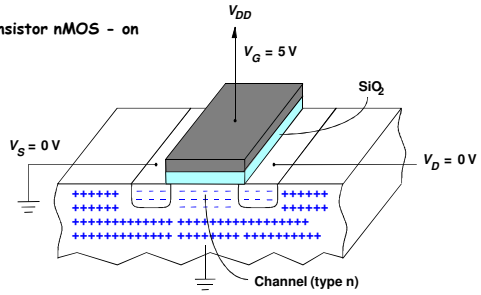
## CMOS: Fabricação e Comportamento

Transistor nMOS - on




When $V_{GS}$ = 5 V, the transistor is on

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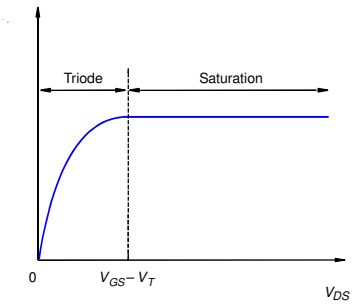
## Transistor nMOS




Current-voltage relationship in the nMOS transistor

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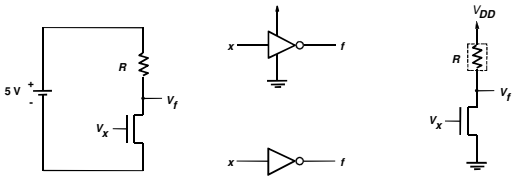
## Portas Lógicas com nMOS




Circuit diagram | Graphical symbols | Simplified circuit diagram

A NOT gate built using nMOS technology

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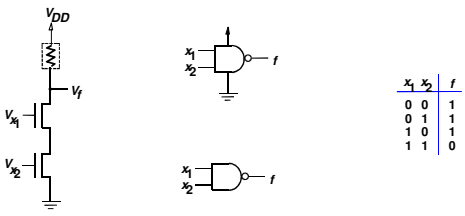
## Portas Lógicas com nMOS (NAND)

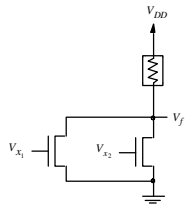



| $x_1$ | $x_2$ | f |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Circuito | Símbolo grafico | Tabela Verdade

MC542 2.35

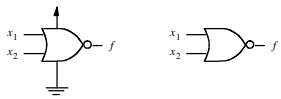
## Portas Lógicas com nMOS (NOR)




(a) Circuit

| $x_1$ | $x_2$ | f |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

(b) Truth table




(c) Graphical symbols

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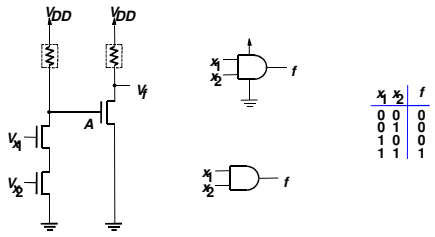
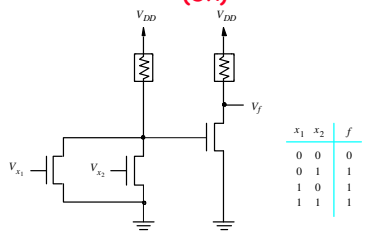
## Portas Lógicas com nMOS (AND)




| $x_1$ | $x_2$ | $f$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

MC542 2.37

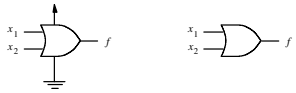
## Portas Lógicas com nMOS (OR)




(a) Circuit

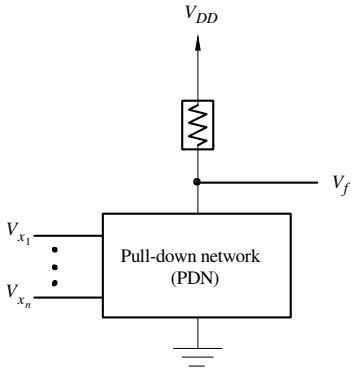
| $x_1$ | $x_2$ | $f$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

(b) Truth table




MC542 2.38

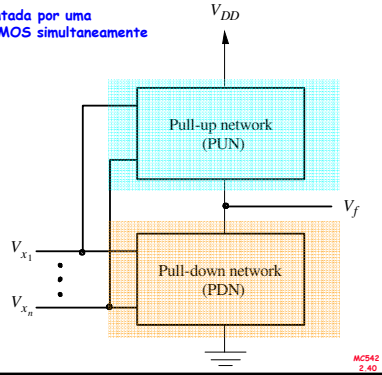
## Estrutura de um Circuito nMOS




MC542 2.39

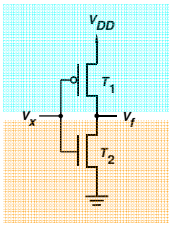
## Estrutura de um Circuito CMOS (nMOS + pMOS)

A função é implementada por uma rede nMOS e uma pMOS simultaneamente




MC542 2.40

## NOT CMOS



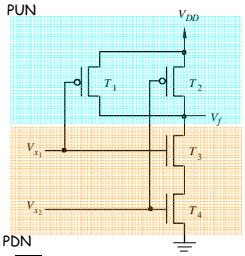

| $x$ | $T_1$ | $T_2$ | $f$ |
|---|---|---|---|
| 0 | on | off | 1 |
| 1 | off | on | 0 |

MC542 2.41

## NAND CMOS

$f = \overline{x_1} + \overline{x_2}$

PUN




PDN

$f = \overline{x_1 . x_2}$

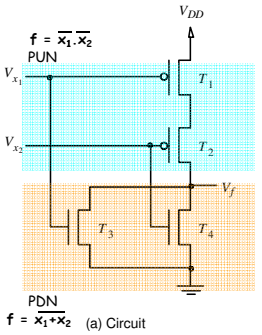
(a) Circuit

| $x_1$ | $x_2$ | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $f$ |
|---|---|---|---|---|---|---|
| 0 | 0 | on | on | off | off | 1 |
| 0 | 1 | on | off | off | on | 1 |
| 1 | 0 | off | on | on | off | 1 |
| 1 | 1 | off | off | on | on | 0 |

(b) Truth table and transistor states

MC542 2.42

## NOR CMOS



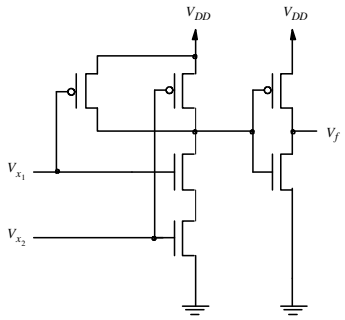

(a) Circuit

| $x_1$ | $x_2$ | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $f$ |
|---|---|---|---|---|---|---|
| 0 | 0 | on | on | off | off | 1 |
| 0 | 1 | on | off | off | on | 0 |
| 1 | 0 | off | on | on | off | 0 |
| 1 | 1 | off | off | on | on | 0 |

(b) Truth table and transistor states

MC542 2.43

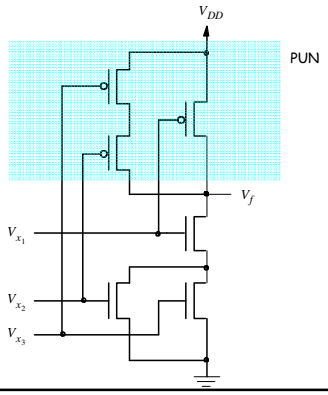
## AND CMOS




MC542 2.44

## Exemplo: Circuito Complexo

f = $\overline{x_1}$ + $\overline{x_2}$ $\overline{x_3}$

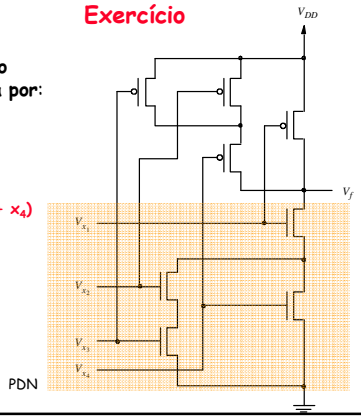



MC542 2.45

## Exercício

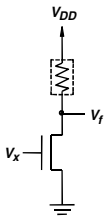
Qual a função implementada por:

$\overline{f}$ = $x_1$ ($x_2x_3$ + $x_4$)

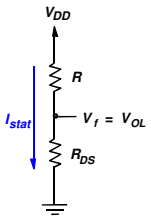



MC542 2.46

## Tensões em um Not nMOS



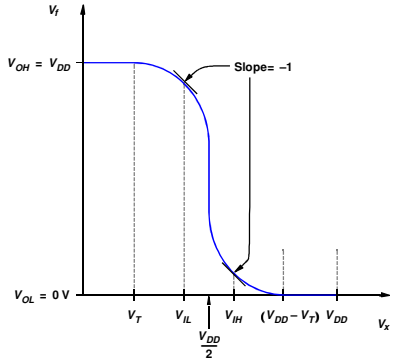

nMOS NOT gate




$V_x$= 5 V

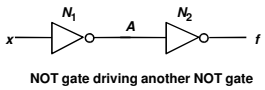
MC542 2.47

## Transferência de Voltagem Not CMOS




MC542 2.48

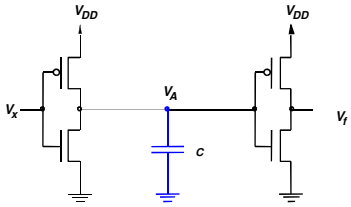
## Margem de Ruído e Capacitância




NOT gate driving another NOT gate

$NM_L = V_{IL} - V_{OL}$

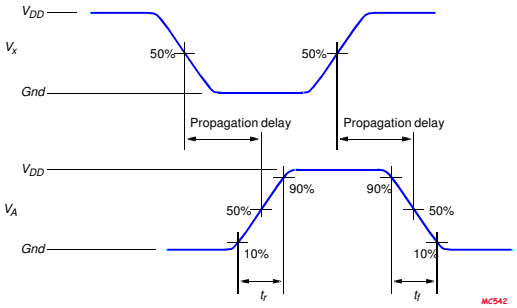
$NM_H = V_{OH} - V_{IH}$




The capacitive load at node A

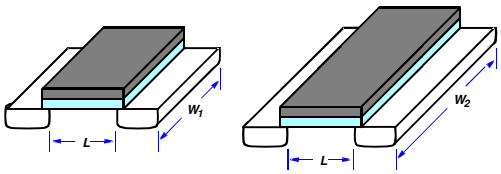
MC542 2.49

## Margem de Ruído e Capacitância




MC542 2.50

## Transistor MOS

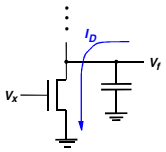



Small transistor

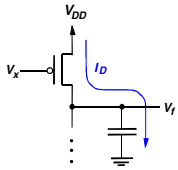
Larger transistor

MC542 2.51

## Consumo de Energia



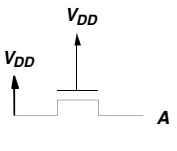

Current flow when input $V_x$ changes from 0 V to 5 V



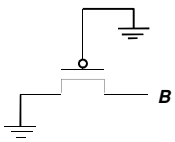

Current flow when input $V_x$ changes from 5 V to 0 V

MC542 2.52

## Passagem de 1s e 0s em MOS



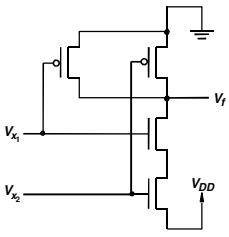

transistor nMOS




transistor pMOS

MC542 2.53

## Implementação "pobre" de um AND CMOS



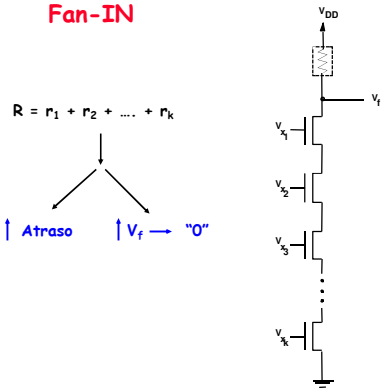

AND gate circuit

| Logic value | | Voltage | Logic value |
|---|---|---|---|
| $x_1$ | $x_2$ | $V_f$ | $f$ |
| 0 | 0 | 1.5 V | 0 |
| 0 | 1 | 1.5 V | 0 |
| 1 | 0 | 1.5 V | 0 |
| 1 | 1 | 3.5 V | 1 |

Truth table and voltage levels

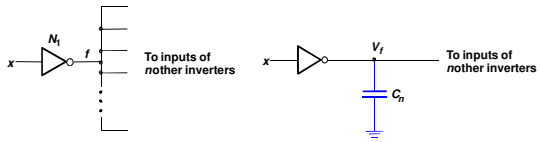
MC542 2.54

## Fan-IN



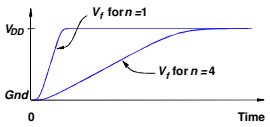

MC542 2.55

## Fan-Out




inverter that drives n other inverters

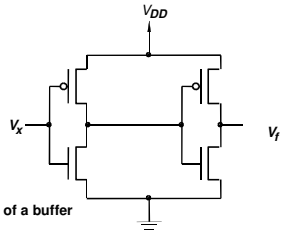
Equivalent circuit for timing purposes



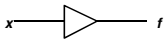

Propagation times for different values of n

MC542 2.56

## Buffer



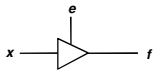

Implementation of a buffer



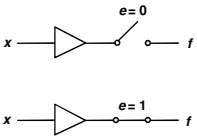

Graphical symbol

MC542 2.57

## Tri-State



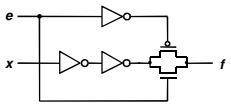

tri-state buffer




Equivalent circuit

| e | x | f |
|---|---|---|
| 0 | 0 | Z |
| 0 | 1 | Z |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

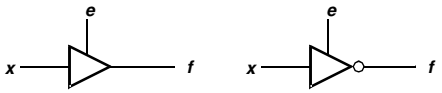
Truth table




Implementation

MC542 2.58

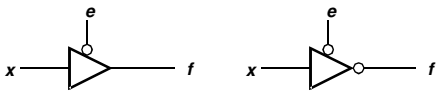
## Tri-State




(a)




(b)



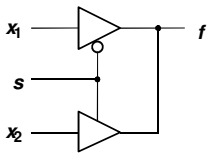

(c)




(d)

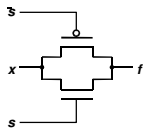
MC542 2.59

## Uso de Tri-State




MC542 2.60

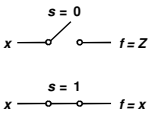
## Transmission Gates




Circuit

| s | f |
|---|---|
| 0 | Z |
| 1 | x |

Truth table




Equivalent circuit

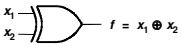

Graphical symbol

MC542
2.61

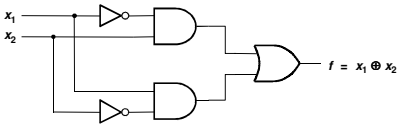
## XOR

| $x_1$ | $x_2$ | $f = x_1 \oplus x_2$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Truth table

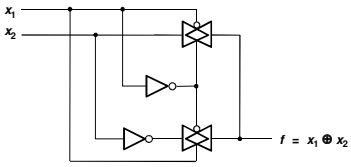



Graphical symbol



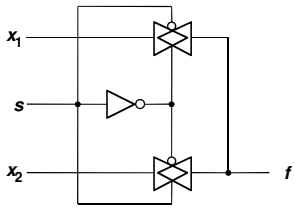

MC542
2.62

## XOR – Transmission Gate




MC542
2.63

## Mux – Transmission Gate




MC542
2.64