

MC542
Organização de Computadores
 Teoria e Prática

2007 - 2011
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MC542
2.1

MC542
Circuitos Lógicos

Portas Lógicas, Tecnologia

"DDCA" - (Capítulo 1)
 "FDL" - (Capítulo 3)

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2.2

Portas Lógicas, Tecnologia
 Sumário

- Variáveis e Funções
 - Funções AND, Or e NOT
 - Funções Complexas
 - Tabela Verdade
- Portas Lógicas
 - Uma Entrada
 - Duas Entradas
 - Múltiplas Entradas
- Rede Lógica
- Níveis Lógicos
 - Margem de Ruído
- Característica de Transferência DC
- Família Lógicas

2.3

Portas Lógicas, Tecnologia
 Sumário

- Transistor como Chave
 - NMOS
 - PMOS
- Portas Lógicas com NMOS
- Portas Lógicas com CMOS
- Fan-In e Fan-Out
- Tri-state
- Transmission Gates

2.4

Variáveis e Funções

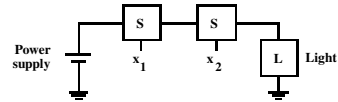
Analogia com chaves controladas

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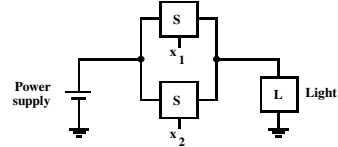
Variáveis e Funções

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Variáveis e Funções - Funções Simples AND e OR



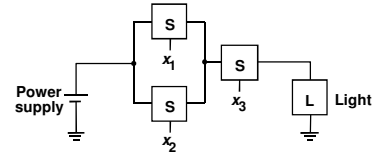
Função lógica AND



Função lógica OR

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2.7

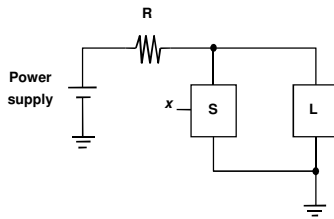
Variáveis e Funções - Funções Complexas



Arranjo serie/paralelo

MCS42
2.8

Variáveis e Funções NOT



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2.9

Tabela Verdade

x_1	x_2	$x_1 \cdot x_2$	$x_1 + x_2$
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

AND OR

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2.10

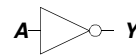
Tabela Verdade

x_1	x_2	x_3	$x_1 \cdot x_2 \cdot x_3$	$x_1 + x_2 + x_3$
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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2.11

Portas Lógicas: Uma Entrada (ou Gates)

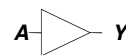
NOT



$$Y = \bar{A}$$

A	Y
0	1
1	0

BUF

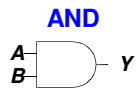


$$Y = A$$

A	Y
0	0
1	1

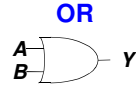
MCS42
2.12

Portas Lógicas: Duas Entradas



$$Y = AB$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



$$Y = A + B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

MCS42 2.13

Portas Lógicas: Duas Entradas



$$Y = A \oplus B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



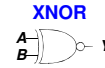
$$Y = \overline{AB}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



$$Y = \overline{A + B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



$$Y = \overline{A \oplus B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

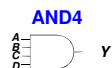
MCS42 2.14

Portas Lógicas: Múltiplas Entradas

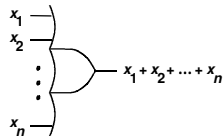


$$Y = \overline{A + B + C}$$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

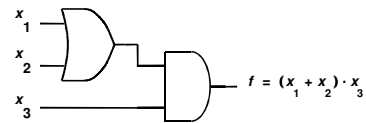


$$Y = ABCD$$



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Rede Lógica



Rede de portas
Circuito lógico

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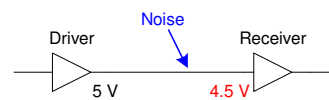
Níveis Lógicos

- Define as voltagens para representar o 1 e o 0
- Exemplo:
 - 0 : terra ou 0 volts
 - 1 : V_{DD} ou 5 volts
- Qual o valor produzido por uma porta (gate)?
- Se produzir 4.99 volts? Isso é um 0 ou um 1?
- E se 3.2 volts?

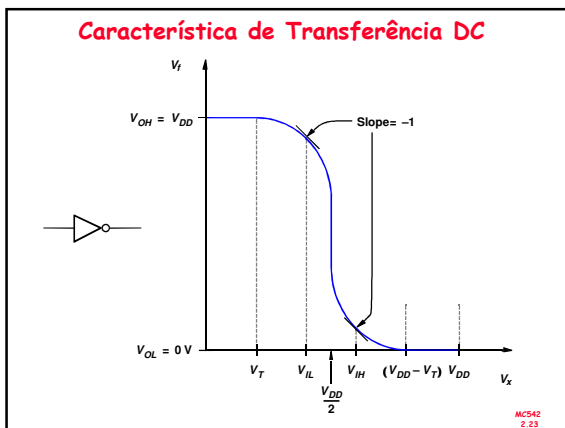
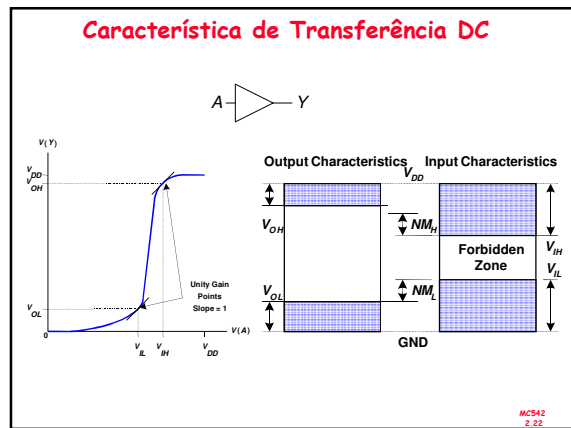
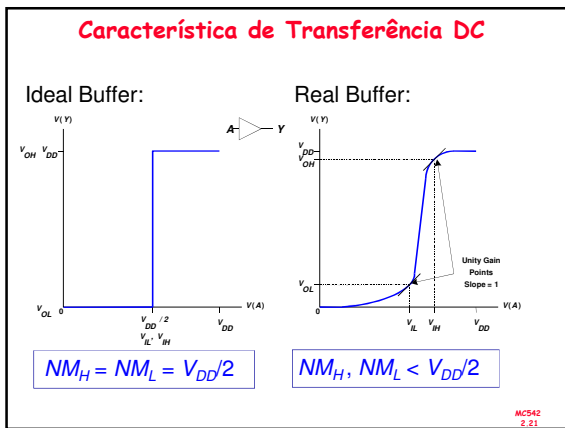
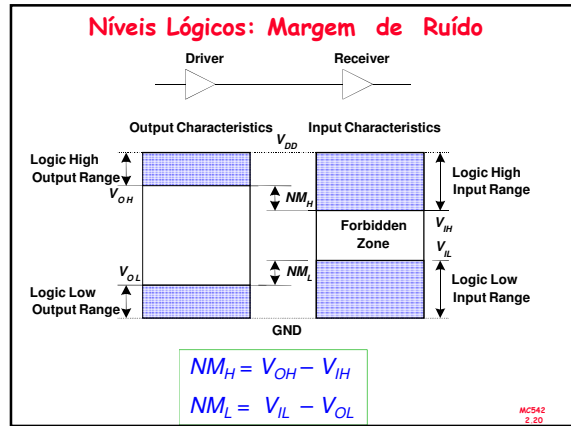
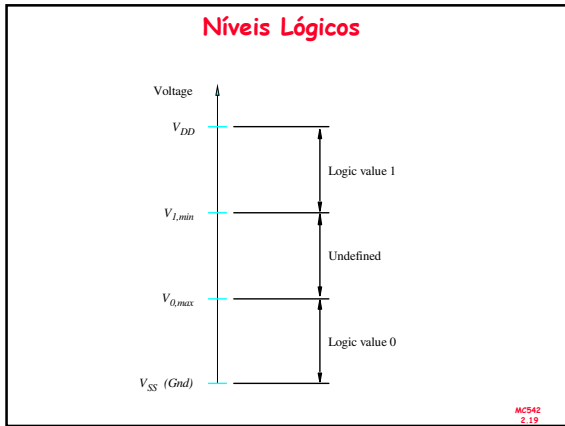
MCS42 2.17

Níveis Lógicos

- Define-se intervalos de voltagens para representar o 1 e o 0
- Define-se diferentes intervalos para saídas e entradas para permitir tolerância a ruídos
- Ruído é qualquer coisa que degrada o sinal



MCS42 2.18



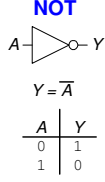
Famílias Lógicas

Logic Family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (4.75 - 5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5 - 6)	1.35	3.15	0.33	3.84
LVTTTL	3.3 (3 - 3.6)	0.8	2.0	0.4	2.4
LVC MOS	3.3 (3 - 3.6)	0.9	1.8	0.36	2.7

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Como Construir as Portas Lógicas

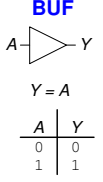
NOT



$Y = \bar{A}$

A	Y
0	1
1	0

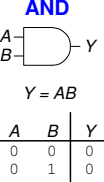
BUF



$Y = A$

A	Y
0	0
1	1

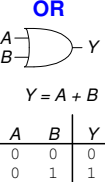
AND



$Y = AB$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR



$Y = A + B$


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Transistores!


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Transistor como Chave

$x = \text{"low"}$

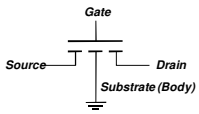


$x = \text{"high"}$



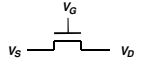
A simple switch controlled by the input x

MOSFET: Metal Oxide Semiconductor Field-Effect Transistor



nMOS transistor

MOSFET: nMOS e pMOS




Simplified symbol for an nMOS transistor

nMOS transistor as a switch


MCS42 2.26

Transistor como Chave

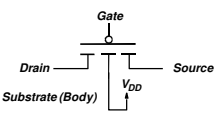
$x = \text{"high"}$



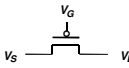
$x = \text{"low"}$



A switch with the opposite behavior of Figure 3.2



pMOS transistor

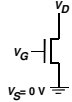


Simplified symbol for a pMOS transistor

pMOS transistor as a switch

MCS42 2.27

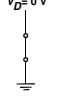
Comportamento dos Transistores NMOS e PMOS em Circuitos



$V_G = 0V$

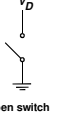
Transistor nMOS

Closed switch when $V_G = V_{DD}$



V_{DD}

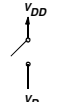
Open switch when $V_G = 0V$



$V_G = V_{DD}$

Transistor pMOS

Open switch when $V_G = V_{DD}$



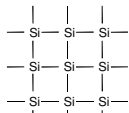
V_{DD}

Closed switch when $V_G = 0V$

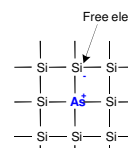
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Transistores

- Transistores são construídos com silício, um semicondutor
- Silício não é condutor (não tem cargas livres)
- Quando dopado torna-se condutor (tem cargas livres)
 - n-type
 - p-type

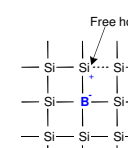


Silicon Lattice



Free electron

n-Type

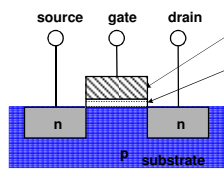


Free hole

p-Type

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Transistor MOS



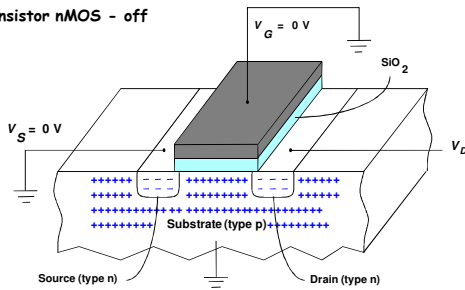
nMOS

pMOS

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CMOS: Fabricação e Comportamento

Transistor nMOS - off

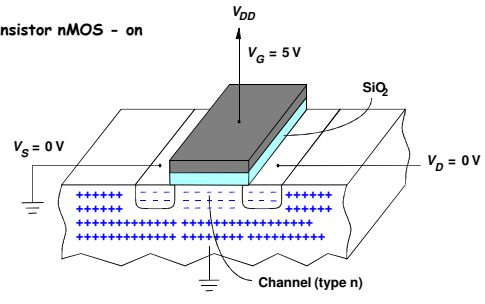


When $V_{GS} = 0$ V, the transistor is off

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2.31

CMOS: Fabricação e Comportamento

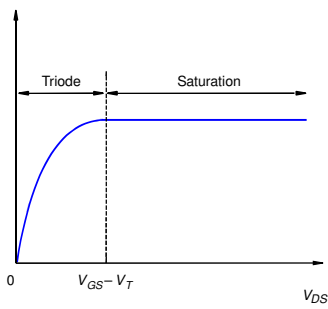
Transistor nMOS - on



When $V_{GS} = 5$ V, the transistor is on

MCS42
2.32

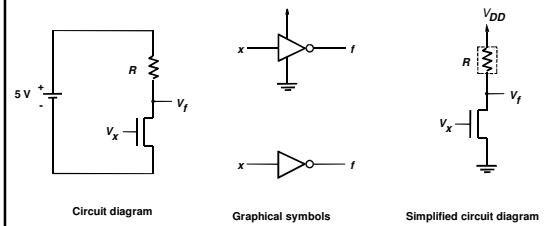
Transistor nMOS



Current-voltage relationship in the nMOS transistor

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2.33

Portas Lógicas com nMOS



Circuit diagram

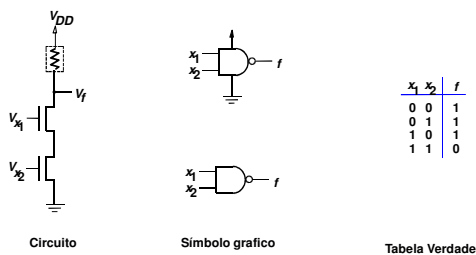
Graphical symbols

Simplified circuit diagram

A NOT gate built using nMOS technology

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2.34

Portas Lógicas com nMOS (NAND)



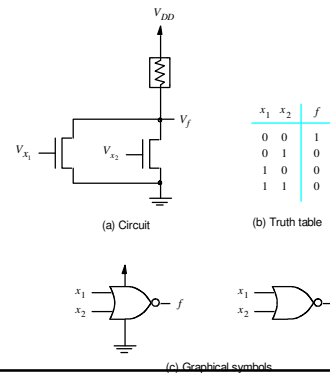
Circuito

Símbolo gráfico

Tabela Verdade

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2.35

Portas Lógicas com nMOS (NOR)



(a) Circuit

(b) Truth table

(c) Graphical symbols

MCS42
2.36

Portas Lógicas com nMOS (AND)

x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

MCS42 2.37

Portas Lógicas com nMOS (OR)

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

MCS42 2.38

Estrutura de um Circuito nMOS

MCS42 2.39

Estrutura de um Circuito CMOS (nMOS + pMOS)

A função é implementada por uma rede nMOS e uma pMOS simultaneamente

MCS42 2.40

NOT CMOS

x	T_1	T_2	f
0	on	off	1
1	off	on	0

MCS42 2.41

NAND CMOS

$f = \overline{x_1 \cdot x_2}$

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(a) Circuit (b) Truth table and transistor states

MCS42 2.42

NOR CMOS

$f = \overline{x_1 \cdot x_2}$

PUN

PDN

$f = \overline{x_1 + x_2}$

(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(b) Truth table and transistor states

MCS42 2.43

AND CMOS

$f = x_1 \cdot x_2$

MCS42 2.44

Exemplo: Circuito Complexo

$f = \overline{x_1} + \overline{x_2} \cdot \overline{x_3}$

PUN

PDN

MCS42 2.45

Exercício

Qual a função implementada por:

$F = x_1 (x_2 x_3 + x_4)$

PUN

PDN

MCS42 2.46

Tensões em um Not nMOS

nMOS NOT gate

$V_x = 5V$

$V_f = V_{OL}$

MCS42 2.47

Transferência de Voltagem Not CMOS

$V_{OH} = V_{DD}$

$V_{OL} = 0V$

Slope = -1

V_T V_{IL} $\frac{V_{DD}}{2}$ V_{IH} $(V_{DD} - V_T)$ V_{DD} V_x

MCS42 2.48

Margem de Ruído e Capacitância

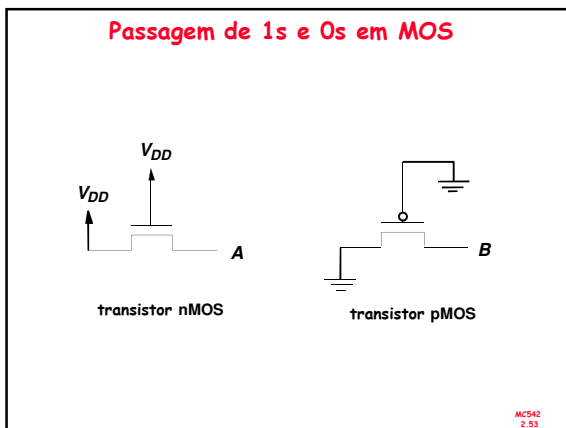
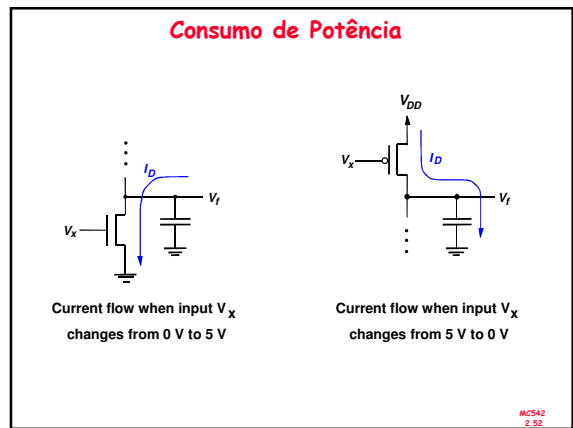
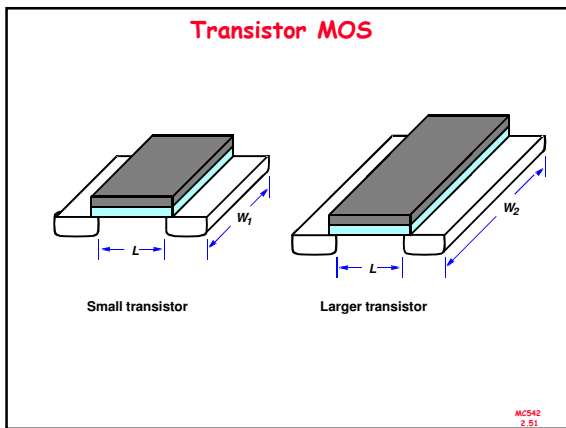
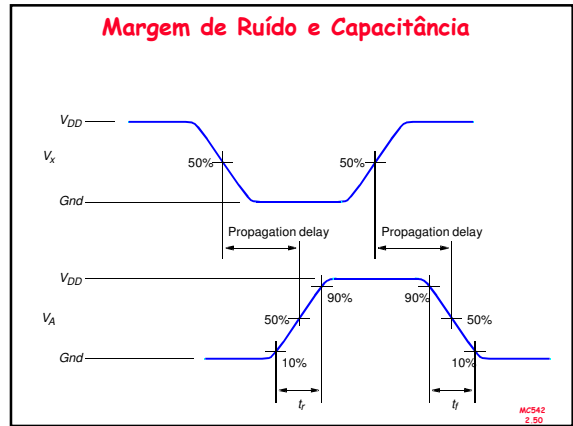
NOT gate driving another NOT gate

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

The capacitive load at node A

MCS42 2.49



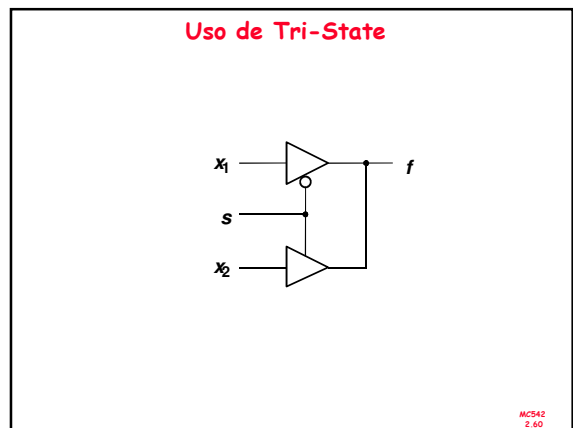
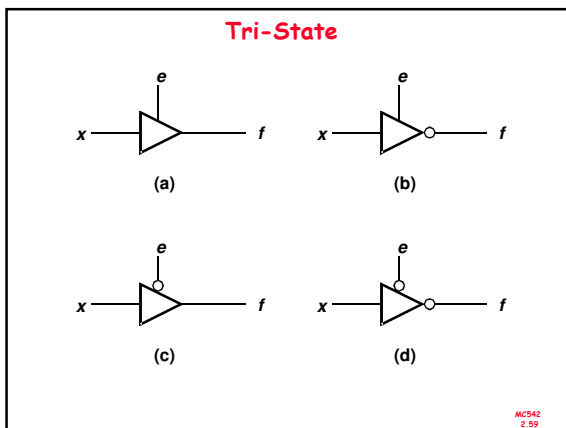
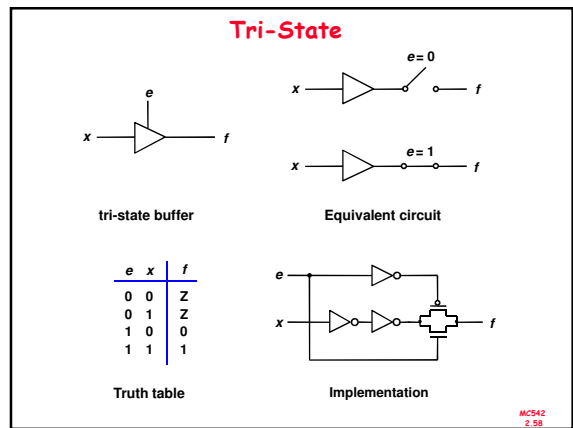
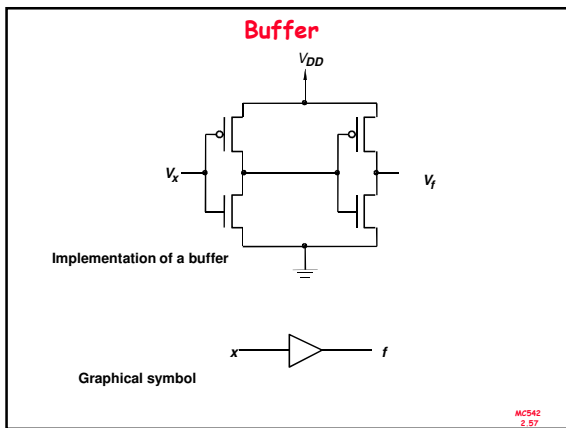
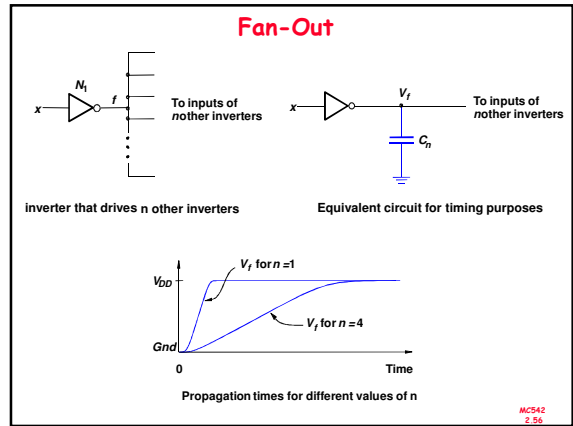
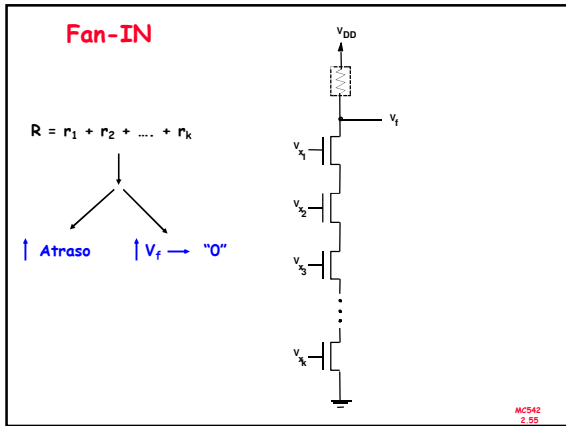
Implementação "pobre" de um AND CMOS

Logic value	Voltage	Logic value
x_1 x_2	V_f	f
0 0	1.5 V	0
0 1	1.5 V	0
1 0	1.5 V	0
1 1	3.5 V	1

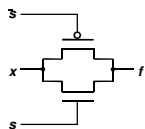
AND gate circuit

Truth table and voltage levels

MCS42 2.54



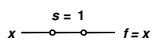
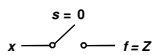
Transmission Gates



Circuit

s	f
0	Z
1	x

Truth table



Equivalent circuit



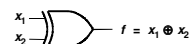
Graphical symbol

MCS42
2.61

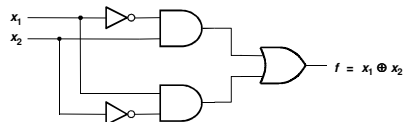
XOR

x_1	x_2	$f = x_1 \oplus x_2$
0	0	0
0	1	1
1	0	1
1	1	0

Truth table

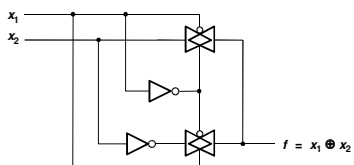


Graphical symbol



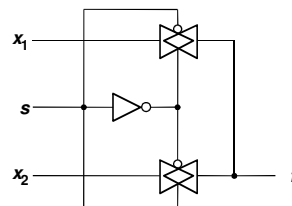
MCS42
2.62

XOR - Transmission Gate



MCS42
2.63

Mux - Transmission Gate



MCS42
2.64