

MC542

Organização de Computadores Teoria e Prática

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MC542

Circuitos Lógicos

Hazards

"Fundamentals of Digital Logic with VHDL Design" - (Capítulo 9.6)

Título do Capítulo Abordado

Sumário

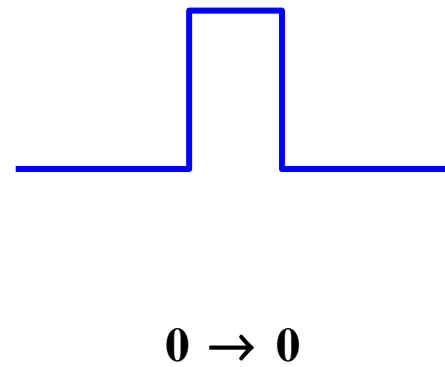
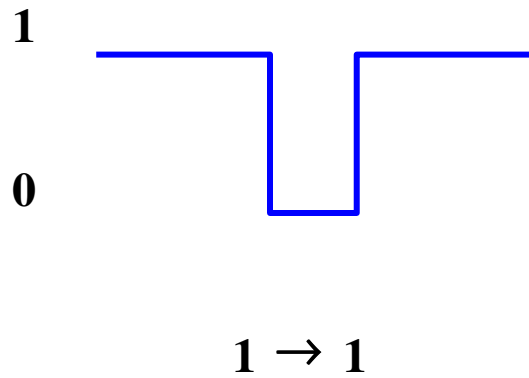
- Hazards
 - Estáticos
 - Dinâmicos

Hazards

- Glitches causados pela estrutura e pelo tempo de propagação em circuitos digitais.
- OBS.: Em circuitos seqüenciais assíncronos é mais prejudicial que em circuitos síncronos.
- Dois tipos de Hazards:
 - Hazard Estático
 - Hazard Dinâmico

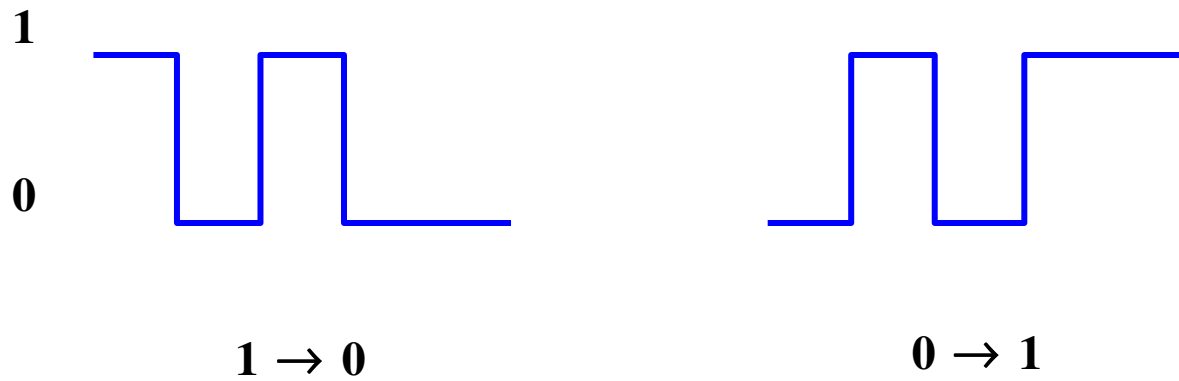
Hazards

- Hazard Estático

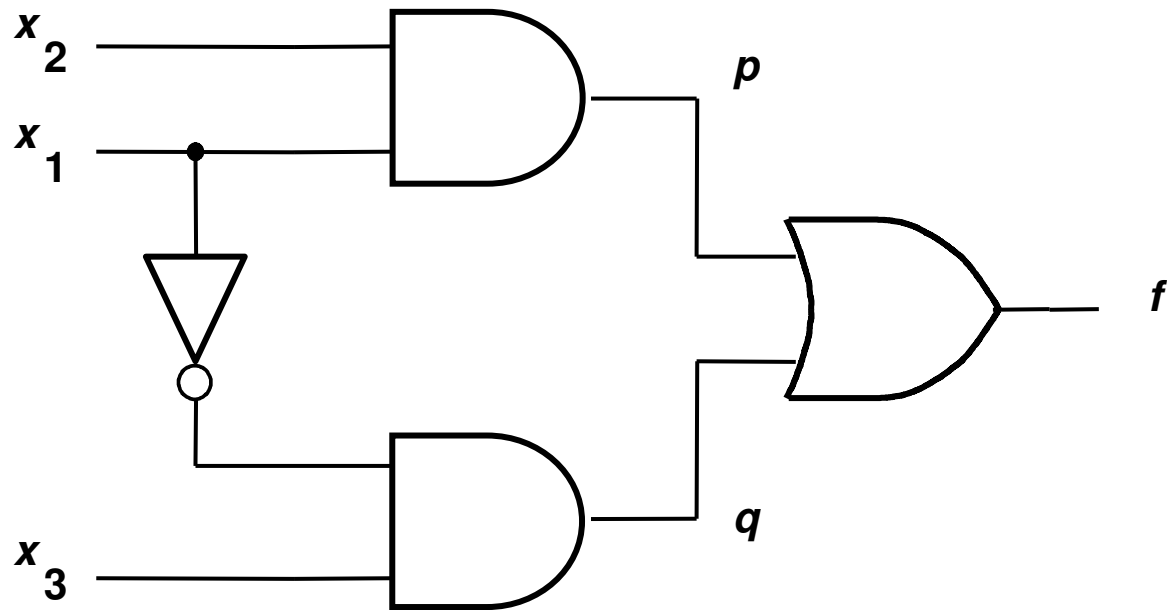


Hazards

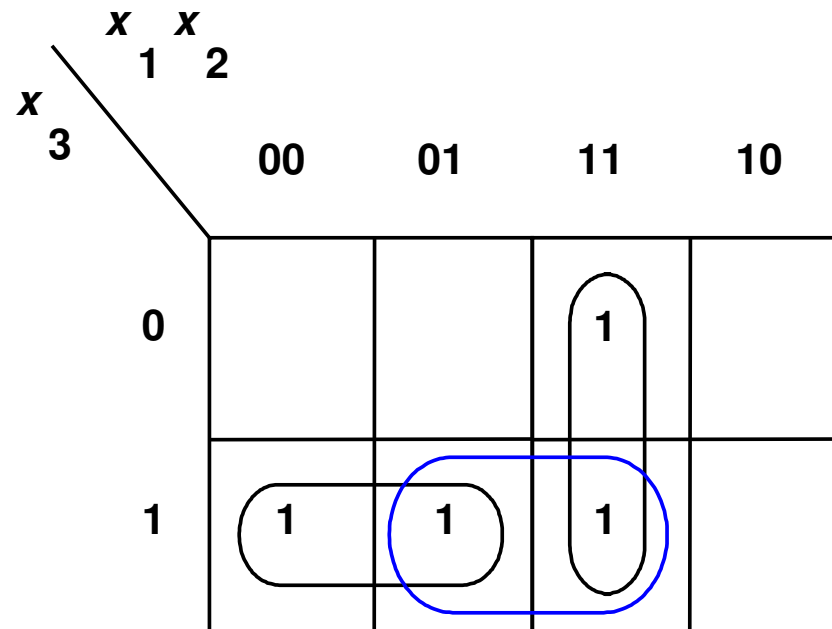
- Hazard Dinâmico



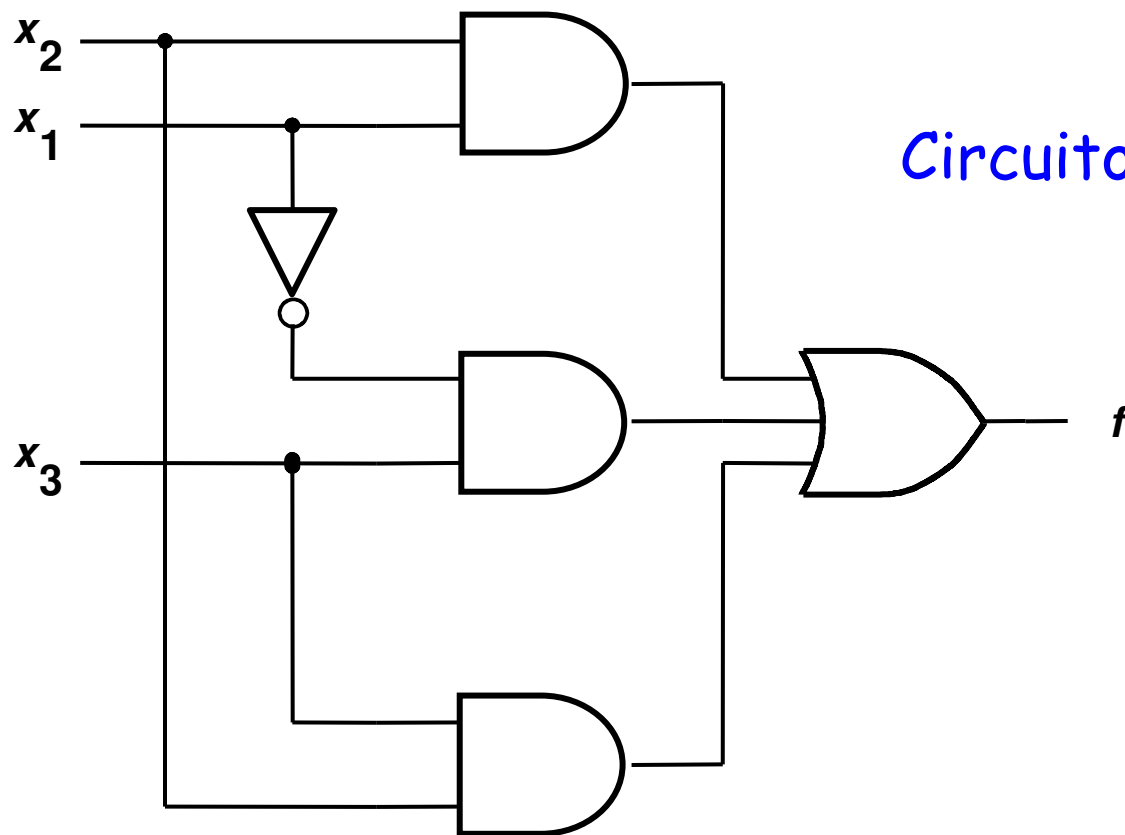
Hazards Estático



Hazards Estático

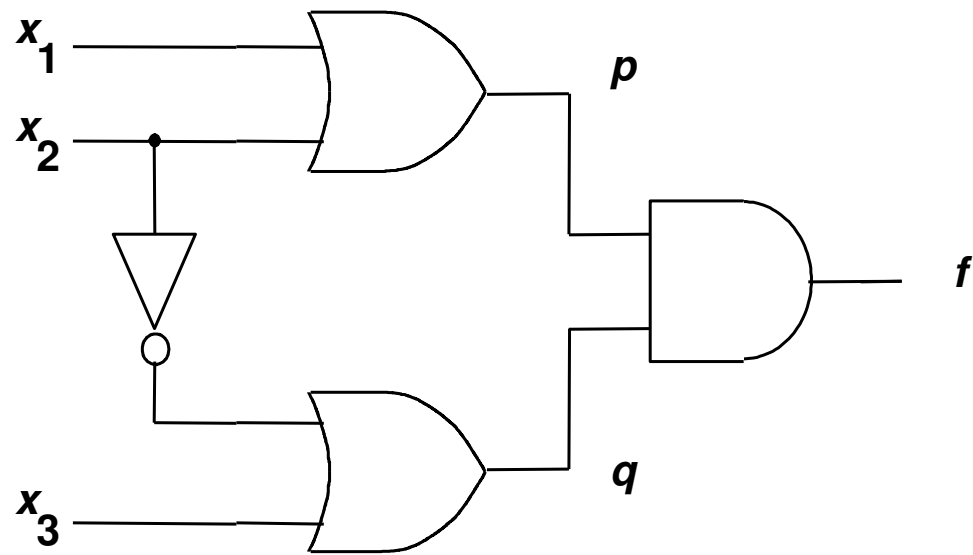


Hazards Estático



Circuito Livre de Hazard

Hazards Estático



Hazards Estático

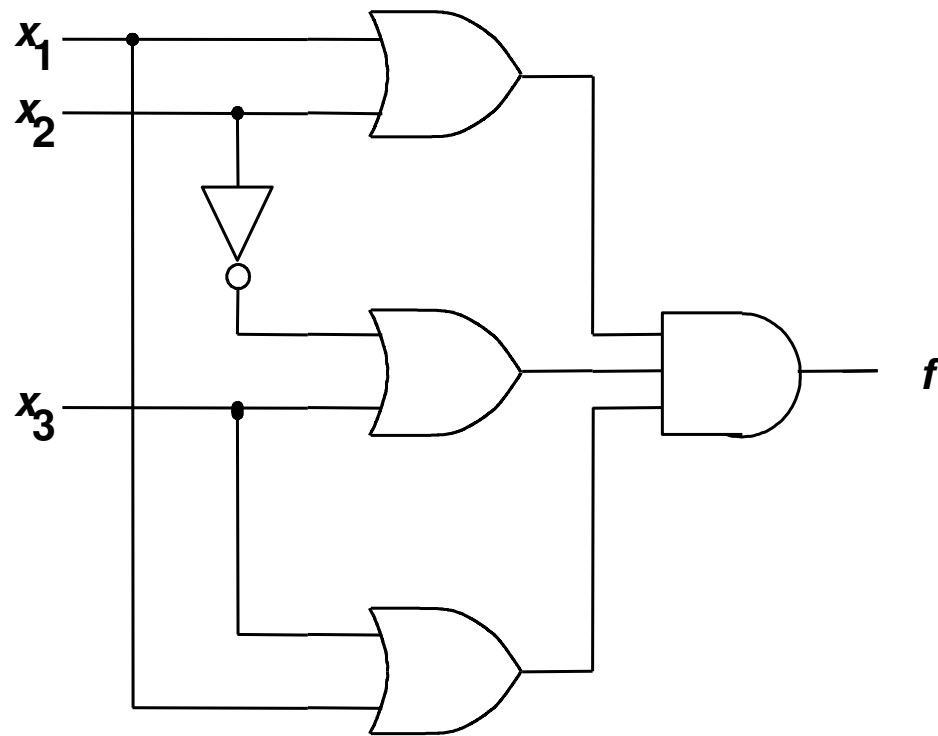
A Karnaugh map for a 3-variable function with variables x_1 , x_2 , and x_3 . The map is a 2x4 grid. The columns are labeled with $x_1 x_2$ values: 00, 01, 11, 10. The rows are labeled with x_3 values: 0, 1. The cells contain the following values:

x_3	$x_1 x_2$ 00	$x_1 x_2$ 01	$x_1 x_2$ 11	$x_1 x_2$ 10
0	0	0	0	1
1	0	1	1	1

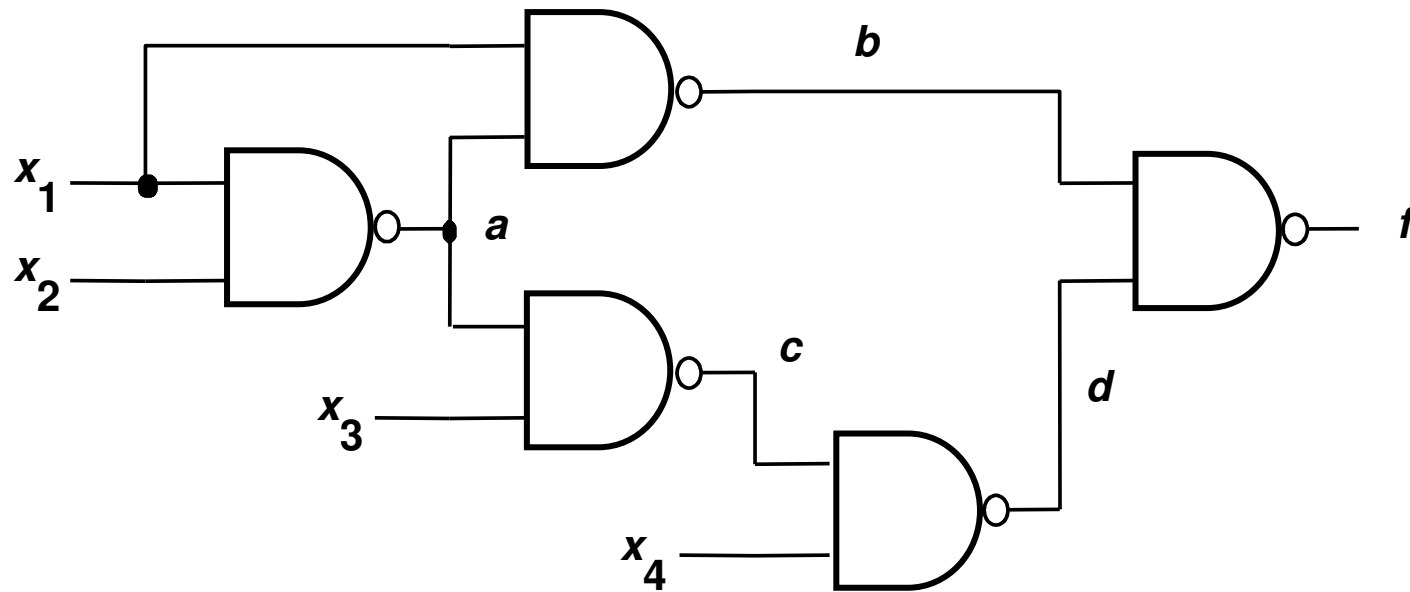
The map shows two prime implicants: a vertical one for $x_3=0$ and a horizontal one for $x_3=0$. A blue circle highlights the hazard between the two prime implicants in the $x_3=0$ row, specifically between the $x_1 x_2$ values 00 and 01.

Hazards Estático

Circuito Livre de Hazard



Hazards Dinâmico



Hazards Dinâmico

