MC542

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MC542

Circuitos Lógicos

Projeto de Circuitos Aritméticos com VHDL

"Fundamentals of Digital Logic with VHDL Design" - (Capítulo 5)

Projeto de Circuitos Aritméticos com VHDL
Sumário

- Circuitos Aritméticos com VHDL

Full-Adder

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY fulladd IS
     PORT ( Cin, x, y  :  IN     STD_LOGIC ;
                 s, Cout   :  OUT  STD_LOGIC ) ;
END fulladd ;

ARCHITECTURE LogicFunc OF fulladd IS
BEGIN
     s <= x XOR y XOR Cin ;
     Cout <= (x AND y) OR (Cin AND x) OR (Cin AND y) ;
END LogicFunc ;
```

Somador de 4 bits

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY adder4 IS
    PORT (  Cin              : IN    STD_LOGIC ;
            x3, x2, x1, x0   : IN    STD_LOGIC ;
            y3, y2, y1, y0   : IN    STD_LOGIC ;
            s3, s2, s1, s0   : OUT   STD_LOGIC ;
            Cout             : OUT   STD_LOGIC ) ;
END adder4 ;

ARCHITECTURE Structure OF adder4 IS
    SIGNAL c1, c2, c3 : STD_LOGIC ;
    COMPONENT fulladd
        PORT (  Cin, x, y    : IN    STD_LOGIC ;
                s, Cout      : OUT   STD_LOGIC ) ;
    END COMPONENT ;
BEGIN
    stage0: fulladd PORT MAP ( Cin, x0, y0, s0, c1 ) ;
    stage1: fulladd PORT MAP ( c1, x1, y1, s1, c2 ) ;
    stage2: fulladd PORT MAP ( c2, x2, y2, s2, c3 ) ;
    stage3: fulladd PORT MAP (
            Cin => c3, Cout => Cout, x => x3, y => y3, s => s3  ) ;
END Structure ;
```

Uso de Package

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

PACKAGE fulladd_package IS
      COMPONENT fulladd
            PORT (   Cin, x, y  : IN       STD_LOGIC ;
                     s, Cout    : OUT      STD_LOGIC ) ;
      END COMPONENT ;
END fulladd_package ;
```

Uso de Package (cont.)

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE work.fulladd_package.all ;

ENTITY adder4 IS
   PORT (Cin              : IN    STD_LOGIC ;
         x3, x2, x1, x0   : IN    STD_LOGIC ;
         y3, y2, y1, y0   : IN    STD_LOGIC ;
         s3, s2, s1, s0   : OUT   STD_LOGIC ;
         Cout             : OUT   STD_LOGIC ) ;
END adder4 ;

ARCHITECTURE Structure OF adder4 IS
   SIGNAL c1, c2, c3 : STD_LOGIC ;
BEGIN
   stage0: fulladd PORT MAP ( Cin, x0, y0, s0, c1 ) ;
   stage1: fulladd PORT MAP ( c1, x1, y1, s1, c2 ) ;
   stage2: fulladd PORT MAP ( c2, x2, y2, s2, c3 ) ;
   stage3: fulladd PORT MAP (
         Cin => c3, Cout => Cout, x => x3, y => y3, s => s3  ) ;
END Structure ;
```

STD_LOGIC_VECTOR

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE work.fulladd_package.all ;

ENTITY adder4 IS
        PORT (Cin   : IN     STD_LOGIC ;
              X, Y : IN     STD_LOGIC_VECTOR(3 DOWNTO 0) ;
              S     : OUT   STD_LOGIC_VECTOR(3 DOWNTO 0) ;
             Cout   : OUT   STD_LOGIC ) ;
END adder4 ;


ARCHITECTURE Structure OF adder4 IS
        SIGNAL C : STD_LOGIC_VECTOR(1 TO 3) ;
BEGIN
        stage0: fulladd PORT MAP ( Cin,  X(0), Y(0), S(0), C(1) ) ;
        stage1: fulladd PORT MAP ( C(1), X(1), Y(1), S(1), C(2) ) ;
        stage2: fulladd PORT MAP ( C(2), X(2), Y(2), S(2), C(3) ) ;
        stage3: fulladd PORT MAP ( C(3), X(3), Y(3), S(3), Cout ) ;
END Structure ;
```

STD_LOGIC_VECTOR

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_signed.all ;

ENTITY adder16 IS
  PORT ( X, Y : IN   STD_LOGIC_VECTOR(15 DOWNTO 0) ;
         S    : OUT  STD_LOGIC_VECTOR(15 DOWNTO 0) ) ;
END adder16 ;

ARCHITECTURE Behavior OF adder16 IS
BEGIN
  S <= X + Y ;
END Behavior ;
```

Perde-se o acesso ao Cout

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_signed.all ;

ENTITY adder16 IS
  PORT (Cin   : IN   STD_LOGIC ;
        X, Y : IN   STD_LOGIC_VECTOR(15 DOWNTO 0) ;
        S     : OUT STD_LOGIC_VECTOR(15 DOWNTO 0) ;
        Cout, Overflow      : OUT STD_LOGIC ) ;
END adder16 ;

ARCHITECTURE Behavior OF adder16 IS
  SIGNAL Sum : STD_LOGIC_VECTOR(16 DOWNTO 0) ;
BEGIN
  Sum <= ('0' & X) + Y + Cin ;
  S <= Sum(15 DOWNTO 0) ;
  Cout <= Sum(16) ;
  Overflow <= Sum(16) XOR X(15) XOR Y(15) XOR Sum(15) ;
END Behavior ;
```

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_arith.all ;

ENTITY adder16 IS
   PORT (       Cin      : IN    STD_LOGIC ;
         X, Y   : IN    SIGNED(15 DOWNTO 0) ;
         S      : OUT   SIGNED(15 DOWNTO 0) ;
         Cout, Overflow : OUT  STD_LOGIC ) ;
END adder16 ;


ARCHITECTURE Behavior OF adder16 IS
   SIGNAL Sum : SIGNED(16 DOWNTO 0) ;
BEGIN
   Sum <= ('0' & X) + Y + Cin ;
   S <= Sum(15 DOWNTO 0) ;
   Cout <= Sum(16) ;
   Overflow <= Sum(16) XOR X(15) XOR Y(15) XOR Sum(15) ;
END Behavior ;
```

INTEGER

```
ENTITY adder16 IS
  PORT (X, Y  : IN   INTEGER RANGE -32768 TO 32767 ;
        S     : OUT  INTEGER RANGE -32768 TO 32767 ) ;
END adder16 ;
```

```
ARCHITECTURE Behavior OF adder16 IS
BEGIN
  S <= X + Y ;
END Behavior ;
```