MC542

Organização de Computadores
Teoria e Prática

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MC542

Circuitos Lógicos

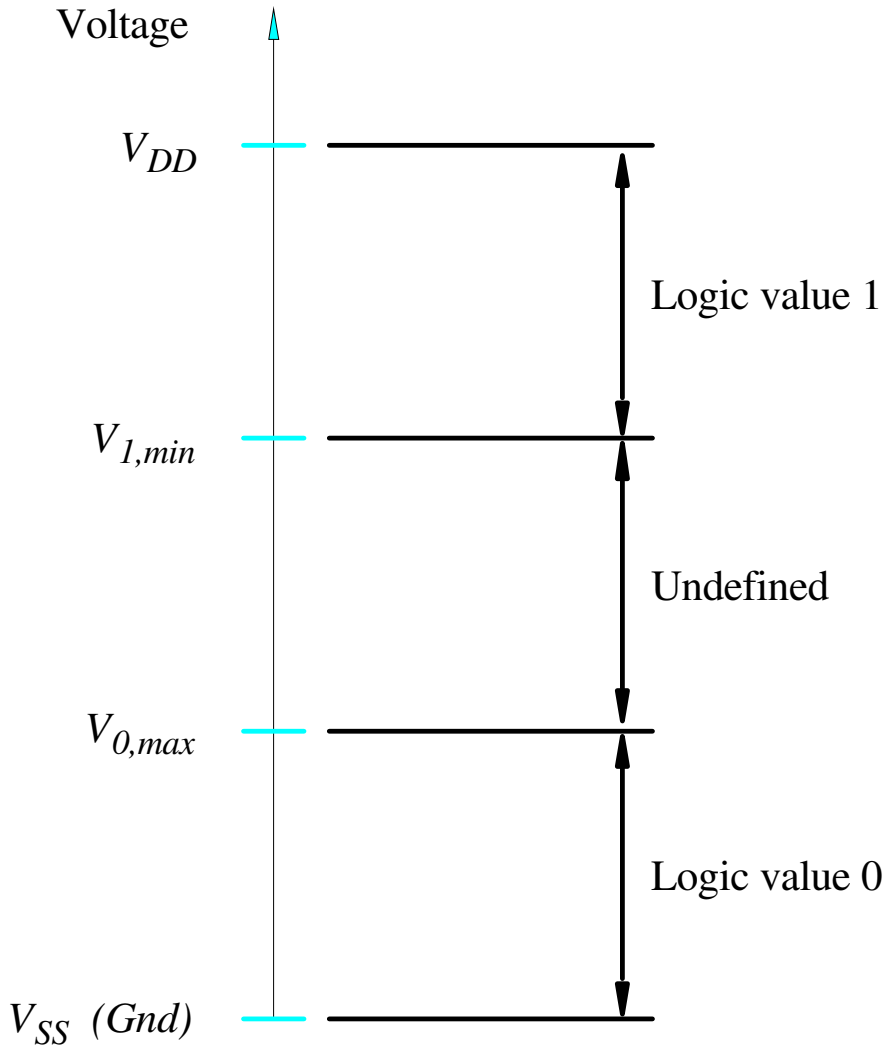
Tecnologia de Implementação

"Fundamentals of Digital Logic with VHDL Design" - (Capítulo 3)

Tecnologia de Implementação
Sumário

- Introdução Transistor Como Chave
- Portas Lógicas NMOS
- Portas Lógicas CMOS
  - Lógica Positiva e Negativa
- Chips Padrões
- Gate Array e FPGAs
- CMOS: Fabricação e Comportamento

Introdução
Valores Lógicos como Voltagem

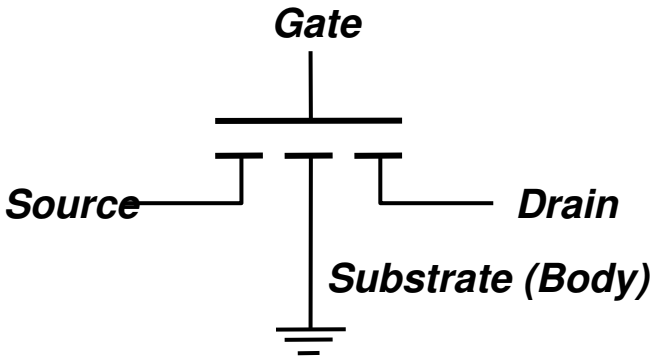


Transistor como Chave

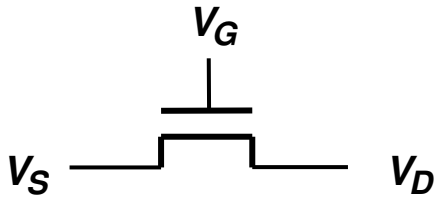
MOSFET: Metal oxide semiconductor field-effect transistor

MOSFET: NMOS e PMOS

A simple switch controlled by the input *x*



NMOS transistor

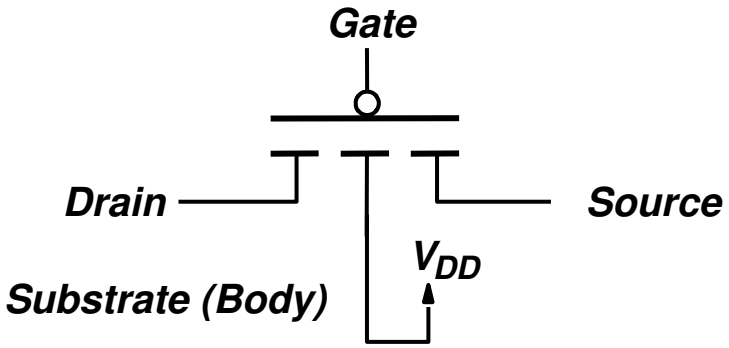


Simplified symbol for an NMOS transistor

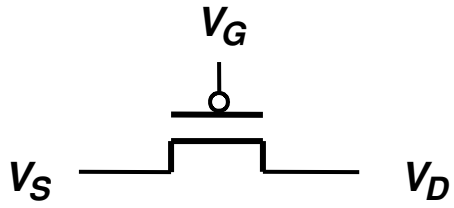
NMOS transistor as a switch

Transistor como Chave

A switch with the opposite behavior of Figure 3.2



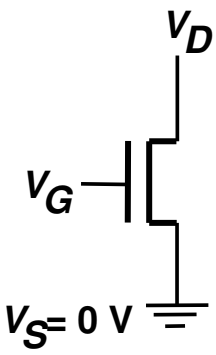
PMOS transistor



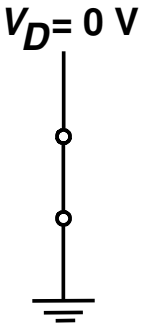
Simplified symbol for an PMOS transistor

PMOS transistor as a switch

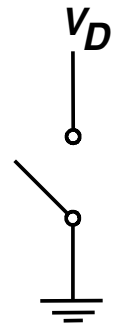
Comportamento dos Transistores NMOS e PMOS em Circuitos



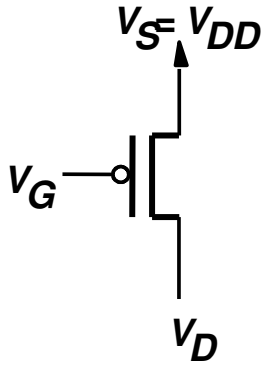
Transistor NMOS



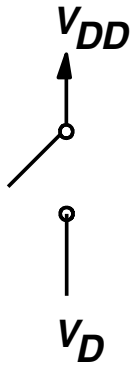
Closed switch
when $V_G = V_{DD}$



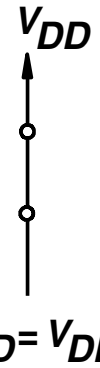
Open switch
when V_G= 0 V



Transistor PMOS

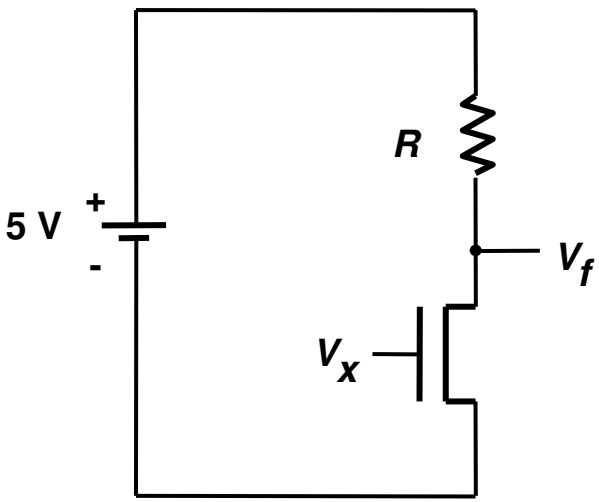


Open switch
when $V_G = V_{DD}$

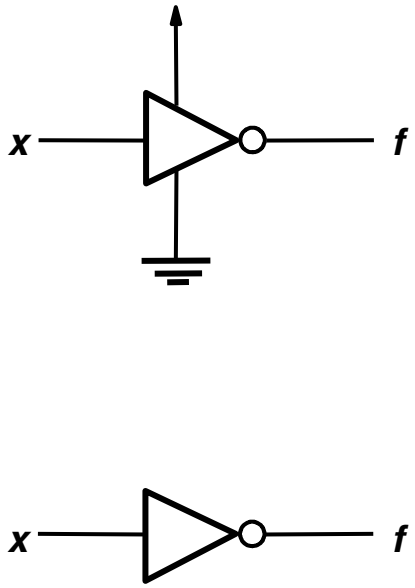


Closed switch
when V_G= 0 V

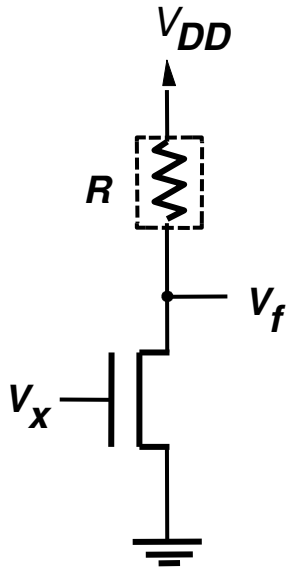
Portas Lógicas com NMOS



Circuit diagram



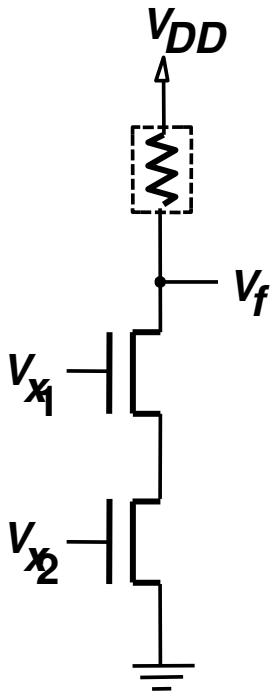
Graphical symbols



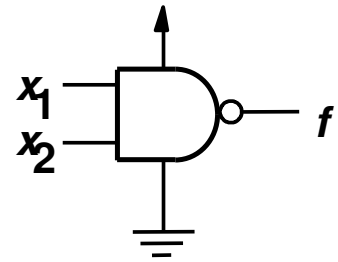
Simplified circuit diagram

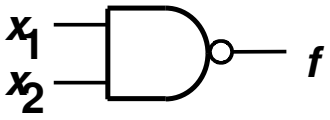
A NOT gate built using NMOS technology

Portas Lógicas com NMOS (NAND)



Circuito



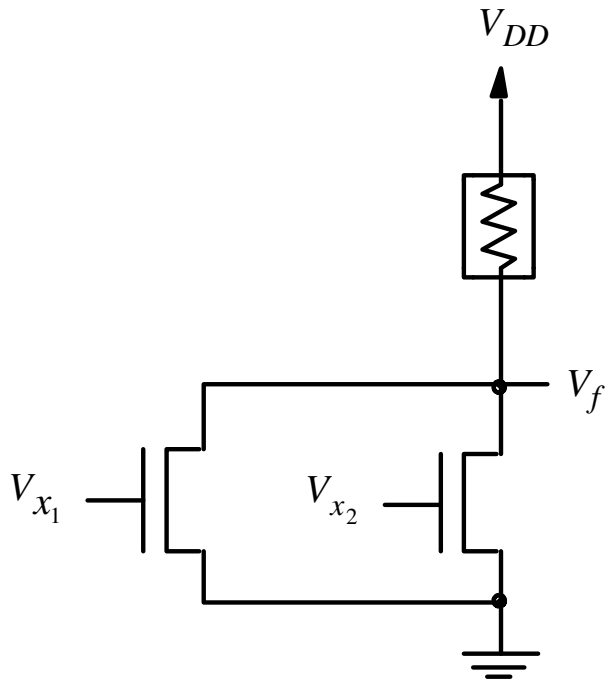


Símbolo grafico

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

Tabela Verdade

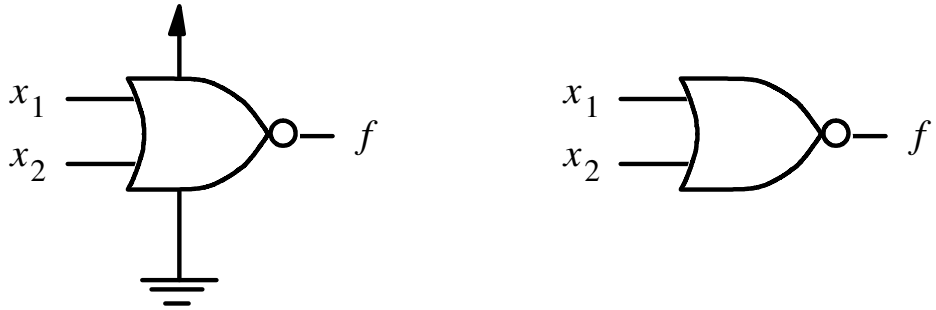
Portas Lógicas com NMOS (NOR)



(a) Circuit

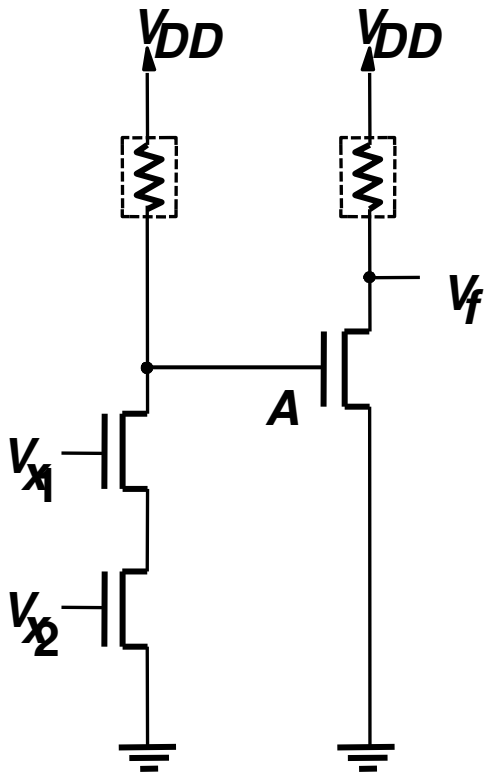
x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

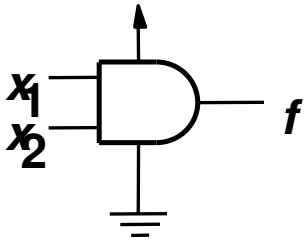
(b) Truth table

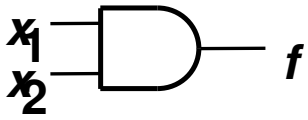


(c) Graphical symbols

Portas Lógicas com NMOS (AND)

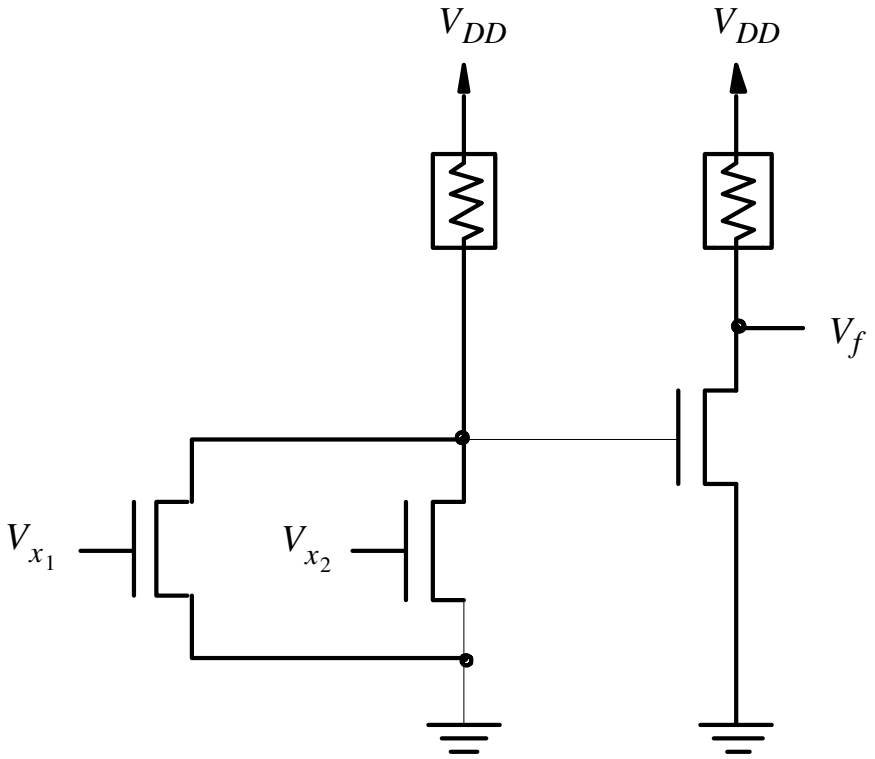






x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

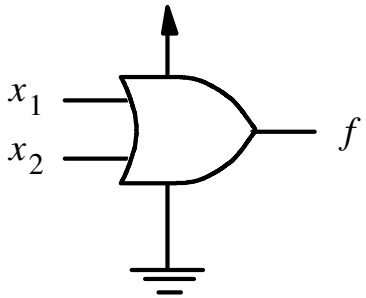
Portas Lógicas com NMOS (OR)

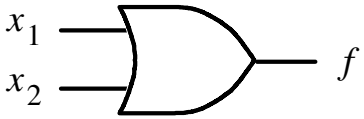


(a) Circuit

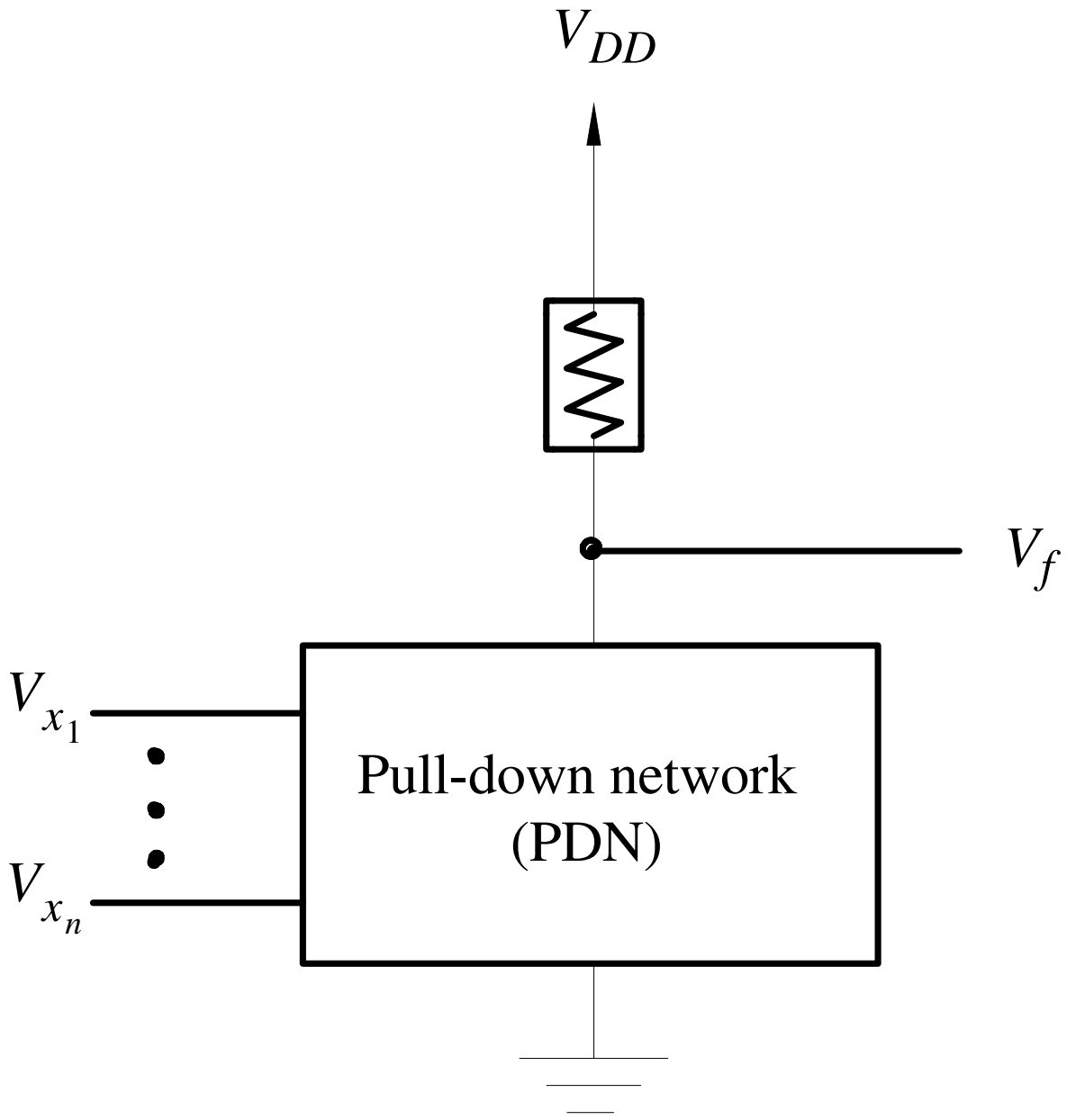
x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table



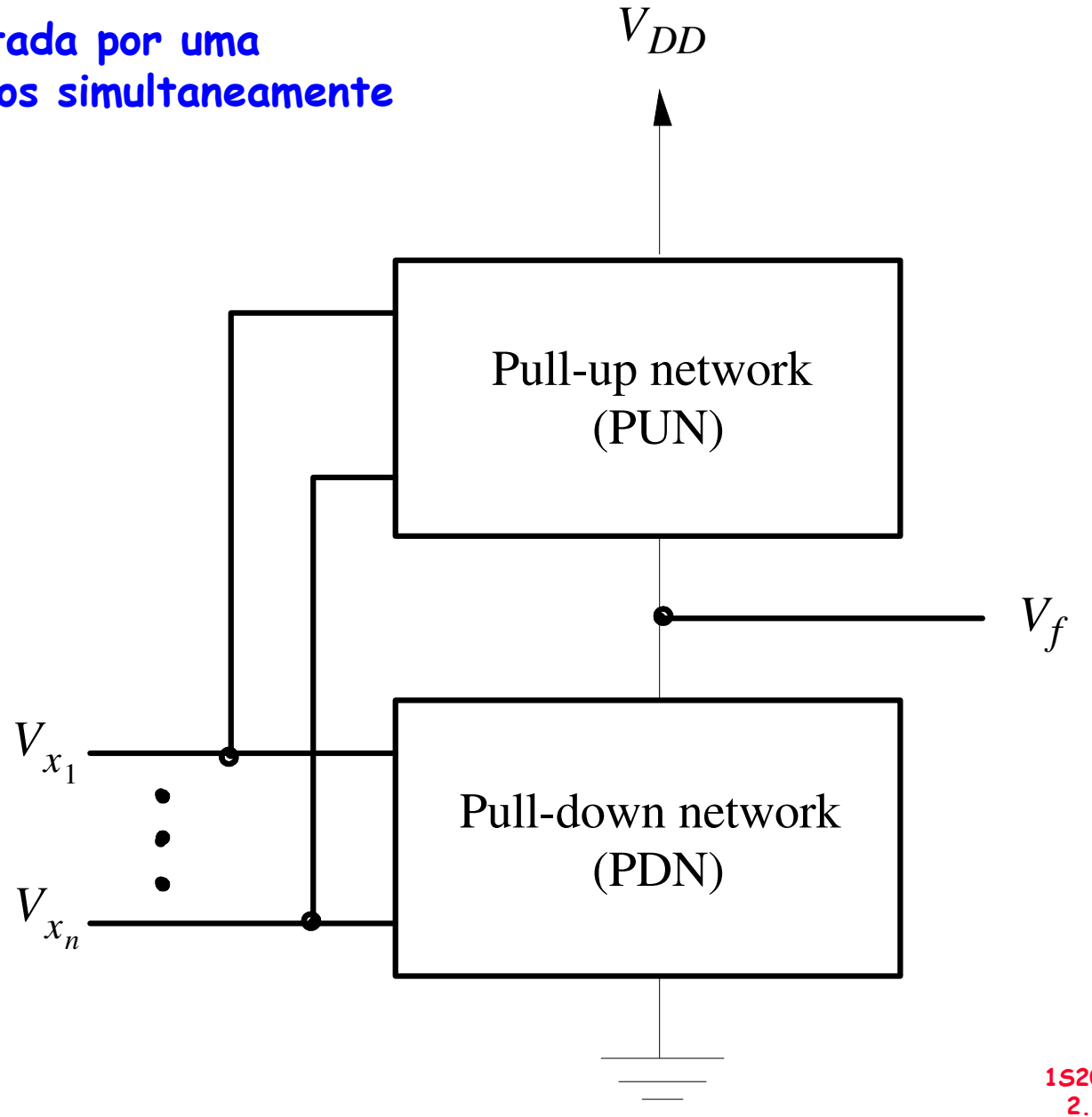


Estrutura de um circuito NMOS

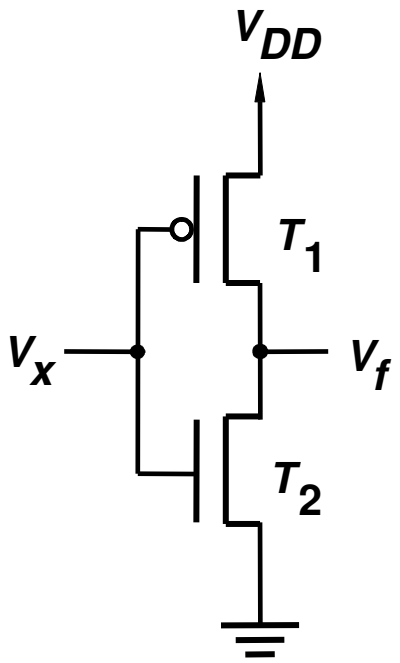


Estrutura de um Circuito CMOS (NMOS + PMOS)

A função é implementada por uma rede Nmos e uma Pmos simultaneamente



NOT CMOS

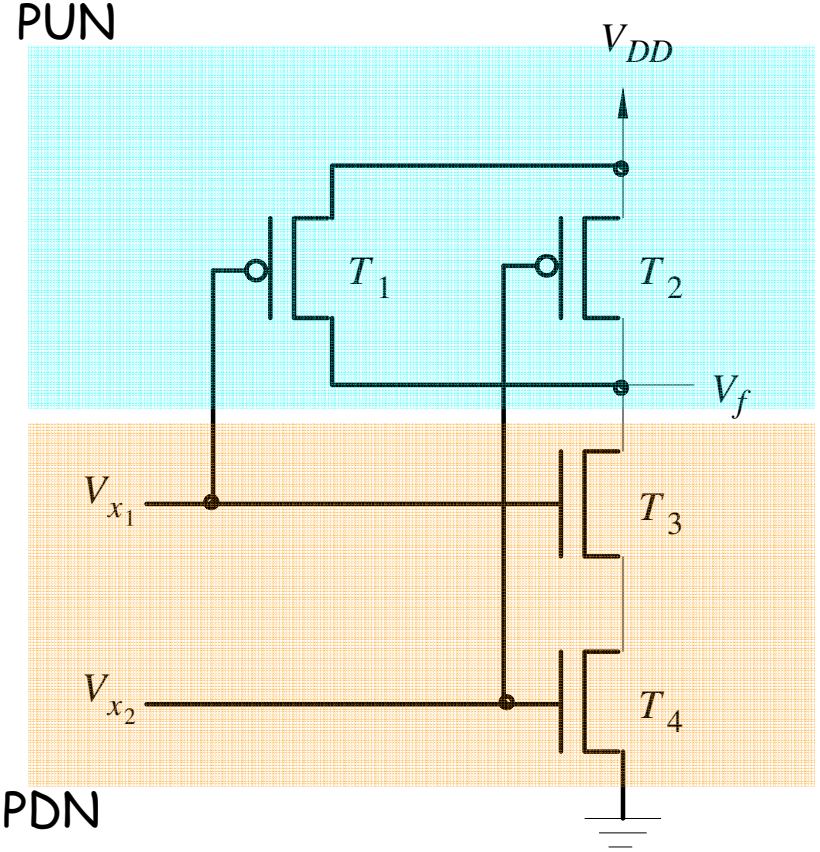


x	T_1	T_2	f
0	on	off	1
1	off	on	0

NAND CMOS

$f = \overline{x_1} + \overline{x_2}$

PUN



PDN

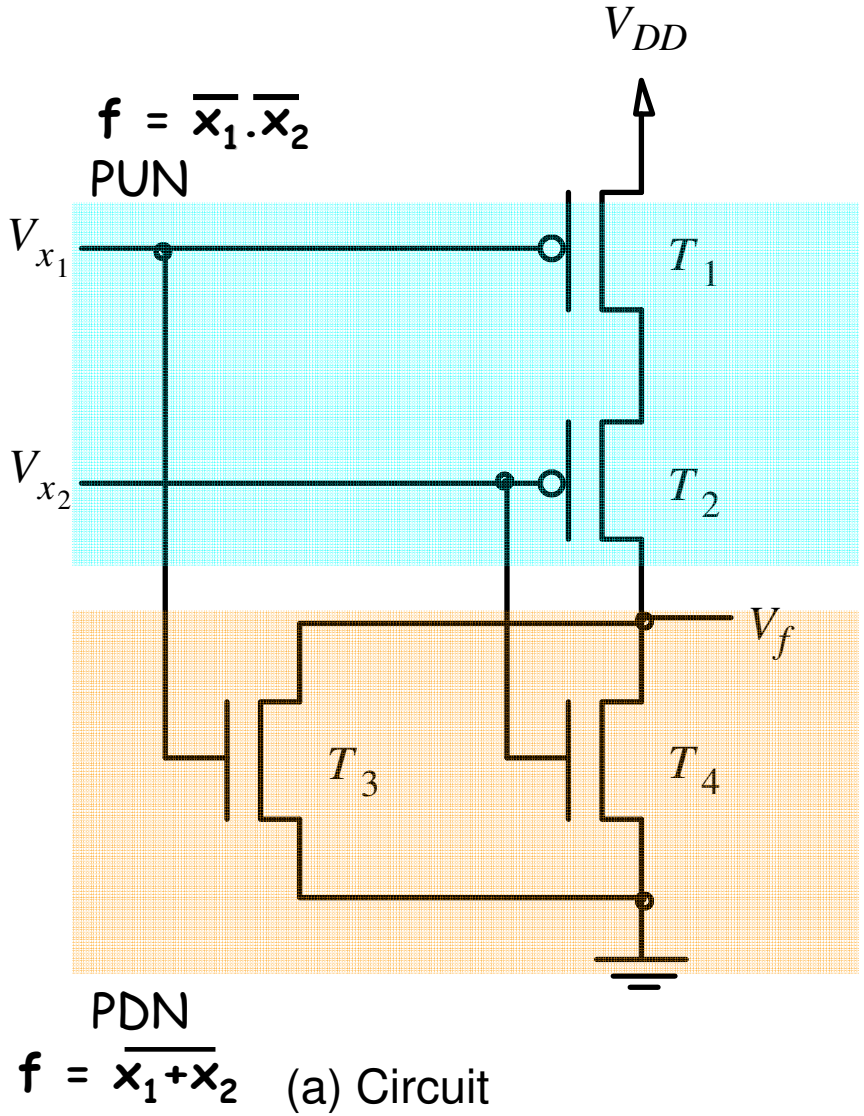
$f = \overline{x_1 . x_2}$

(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

NOR CMOS

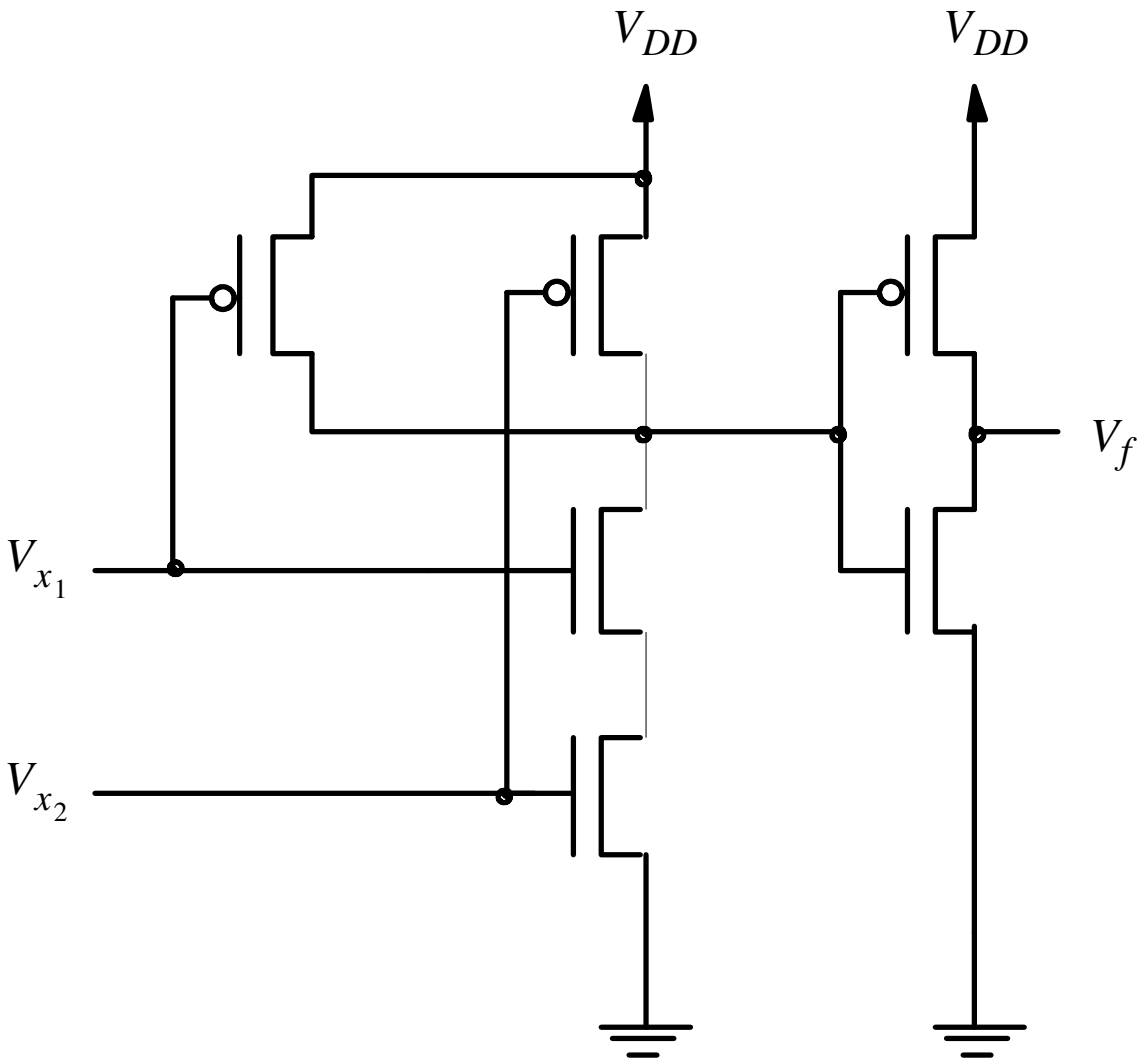


(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

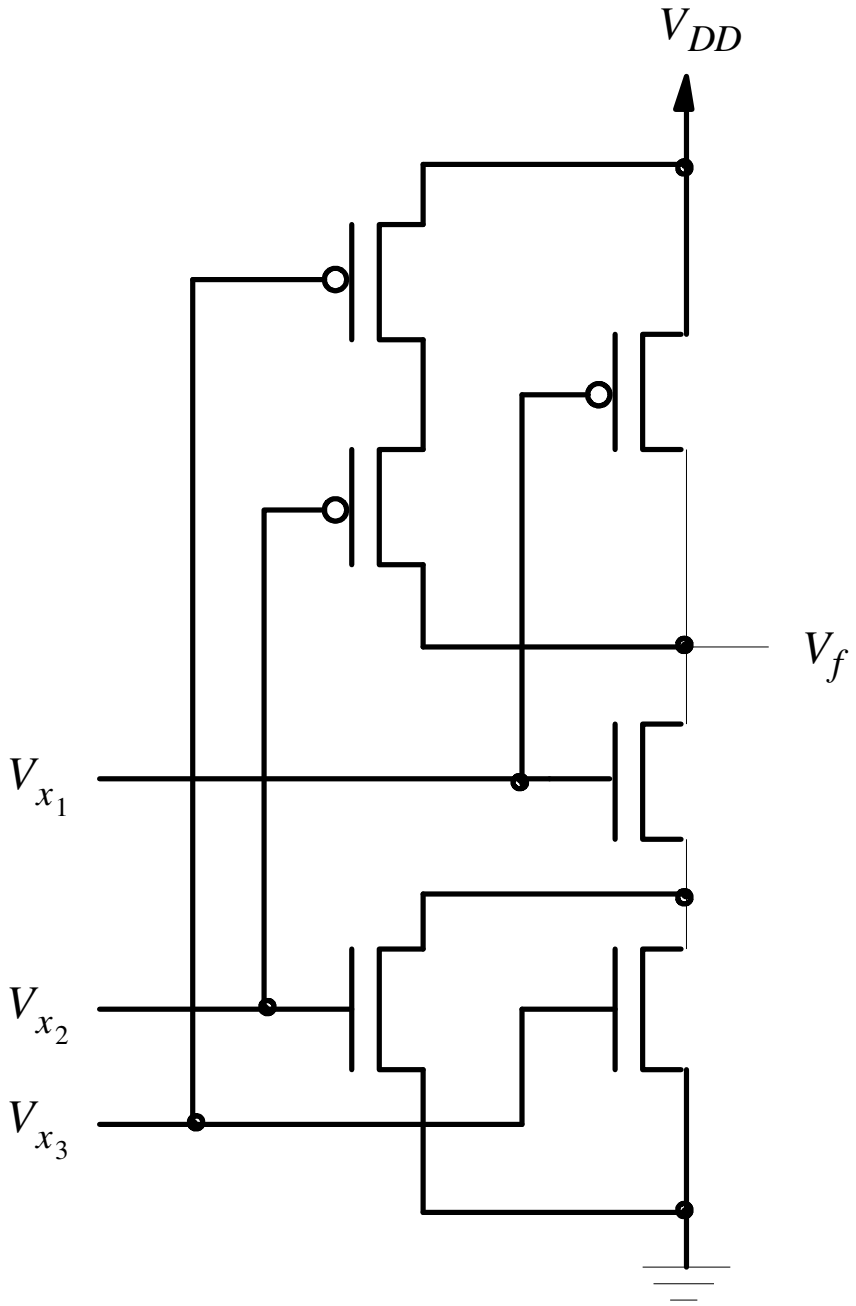
(b) Truth table and transistor states

AND CMOS



Exemplo: Circuito Complexo

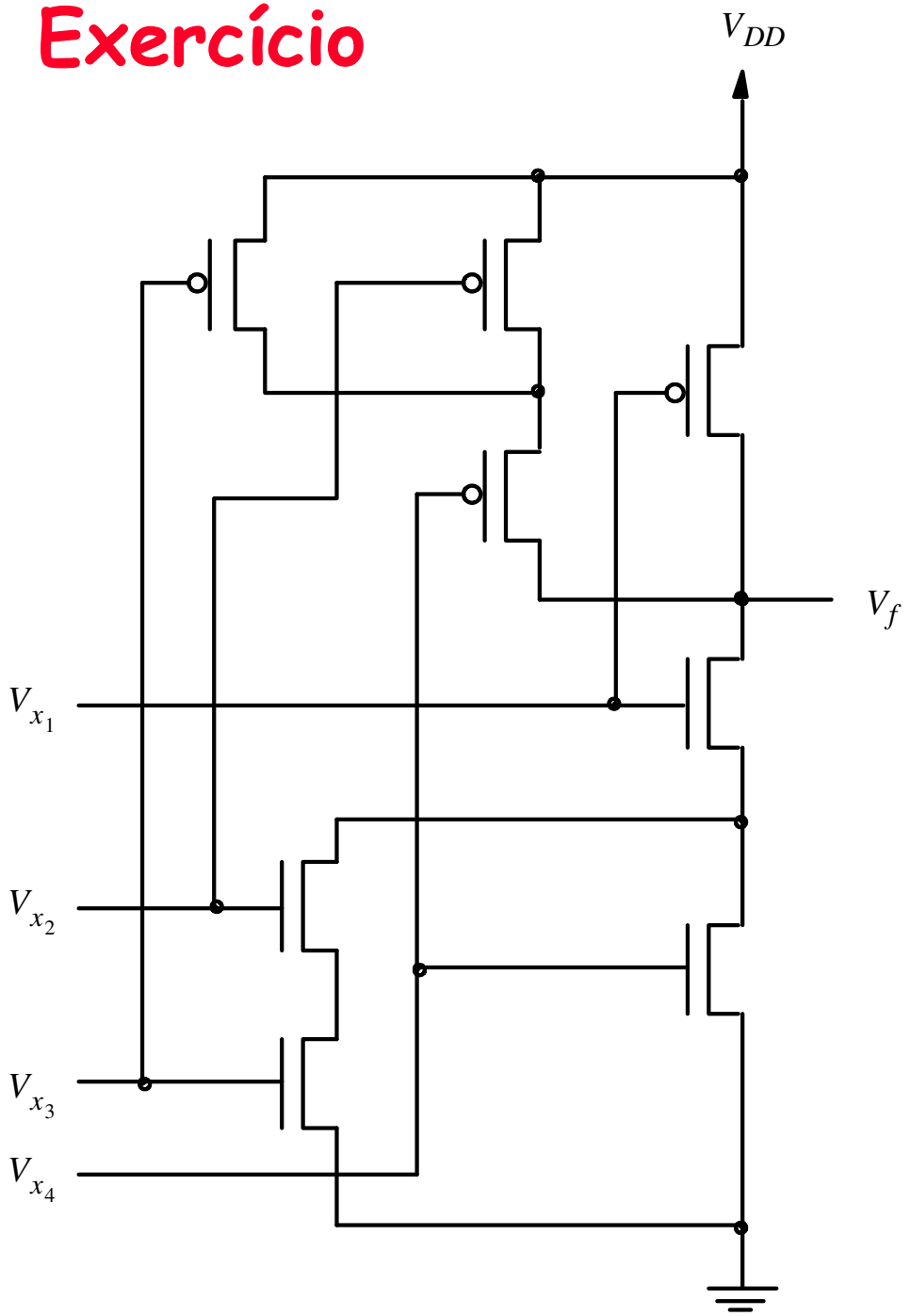
$f = \overline{x_1} + \overline{x_2}\ \overline{x_3}$



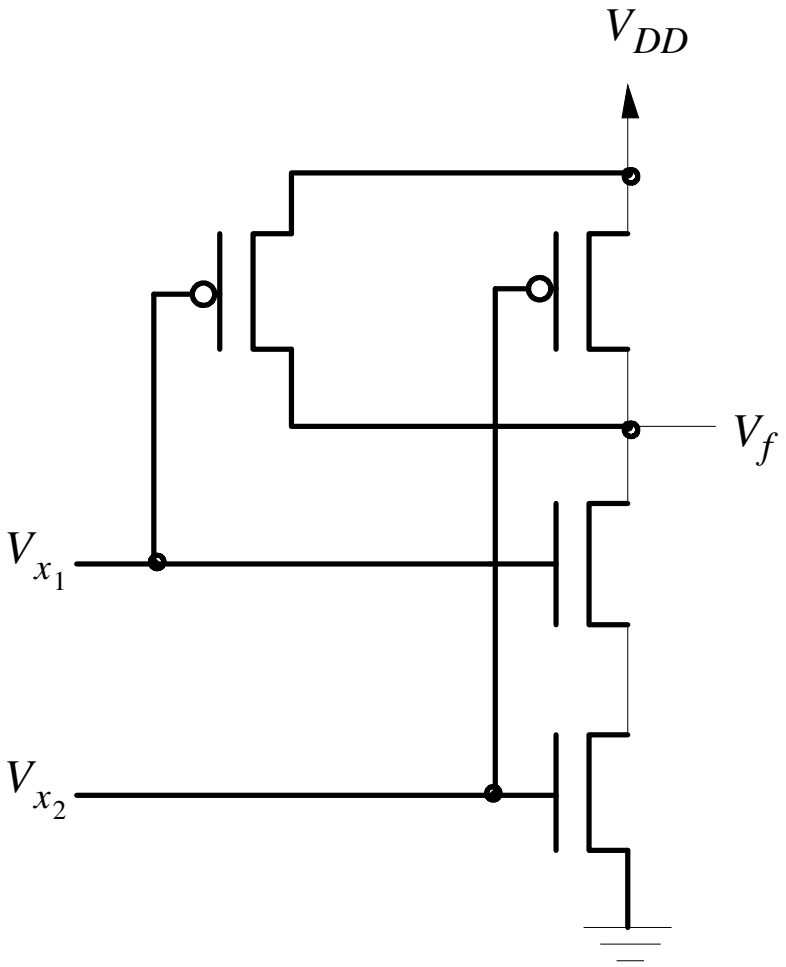
Exercício

Qual a função implementada por:

$$\overline{f} = x_1 (x_2 x_3 + x_4)$$



Níveis de Tensão no Circuito



(a) Circuit

Tensão no circuito

V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

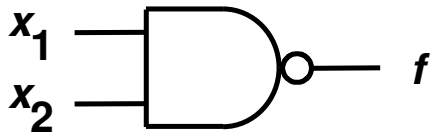
(b) Voltage levels

Lógica Positiva e Negativa

V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

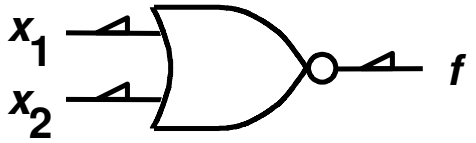
Níveis de Tensão

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0



Logica Positiva: Tabela Verdade e Porta

x_1	x_2	f
1	1	0
1	0	0
0	1	0
0	0	1



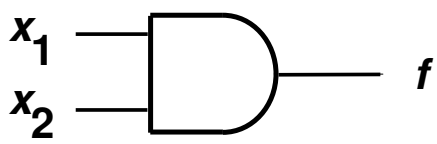
Logica Negativa: Tabela Verdade e Porta

Lógica Positiva e Negativa

V_{x_1}	V_{x_2}	V_f
L	L	L
L	H	L
H	L	L
H	H	H

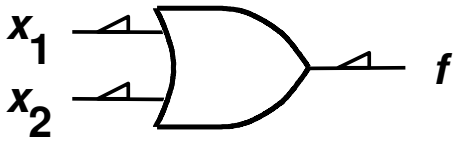
Níveis de Tensão

x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1



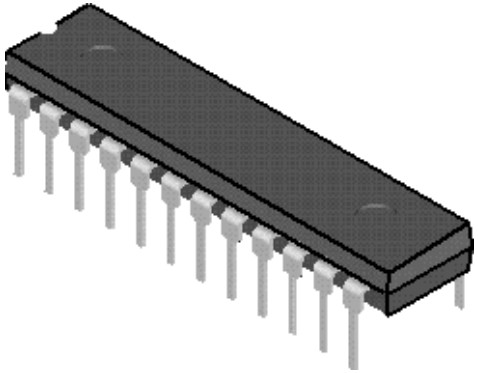
Logica Positiva: Tabela Verdade e Porta

x_1	x_2	f
1	1	1
1	0	1
0	1	1
0	0	0

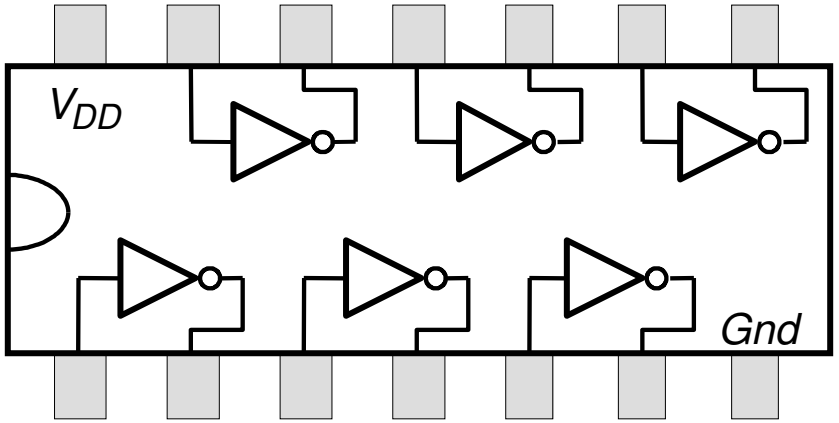


Logica Negativa: Tabela Verdade e Porta

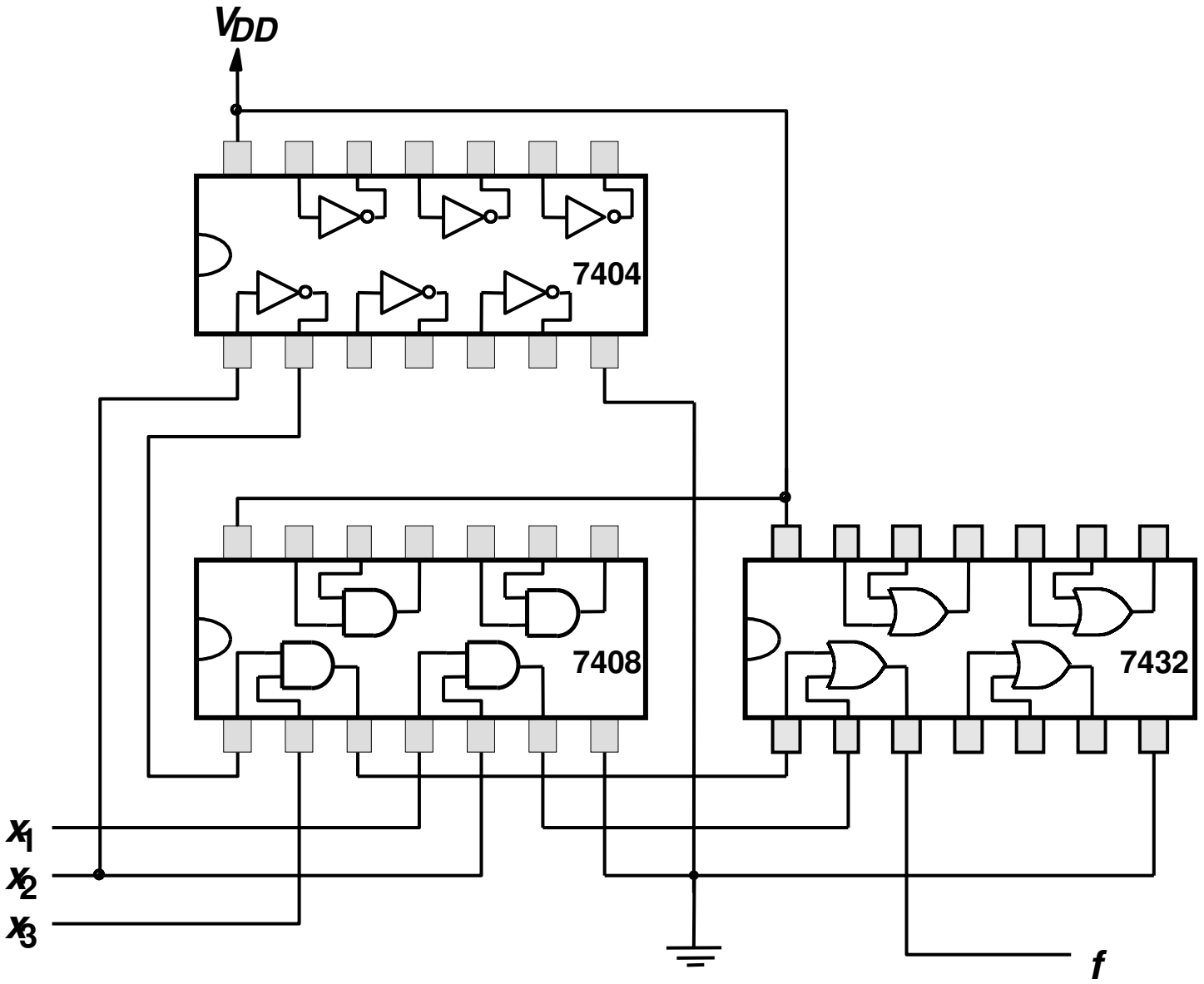
Chips Padrões



Dual-inline package

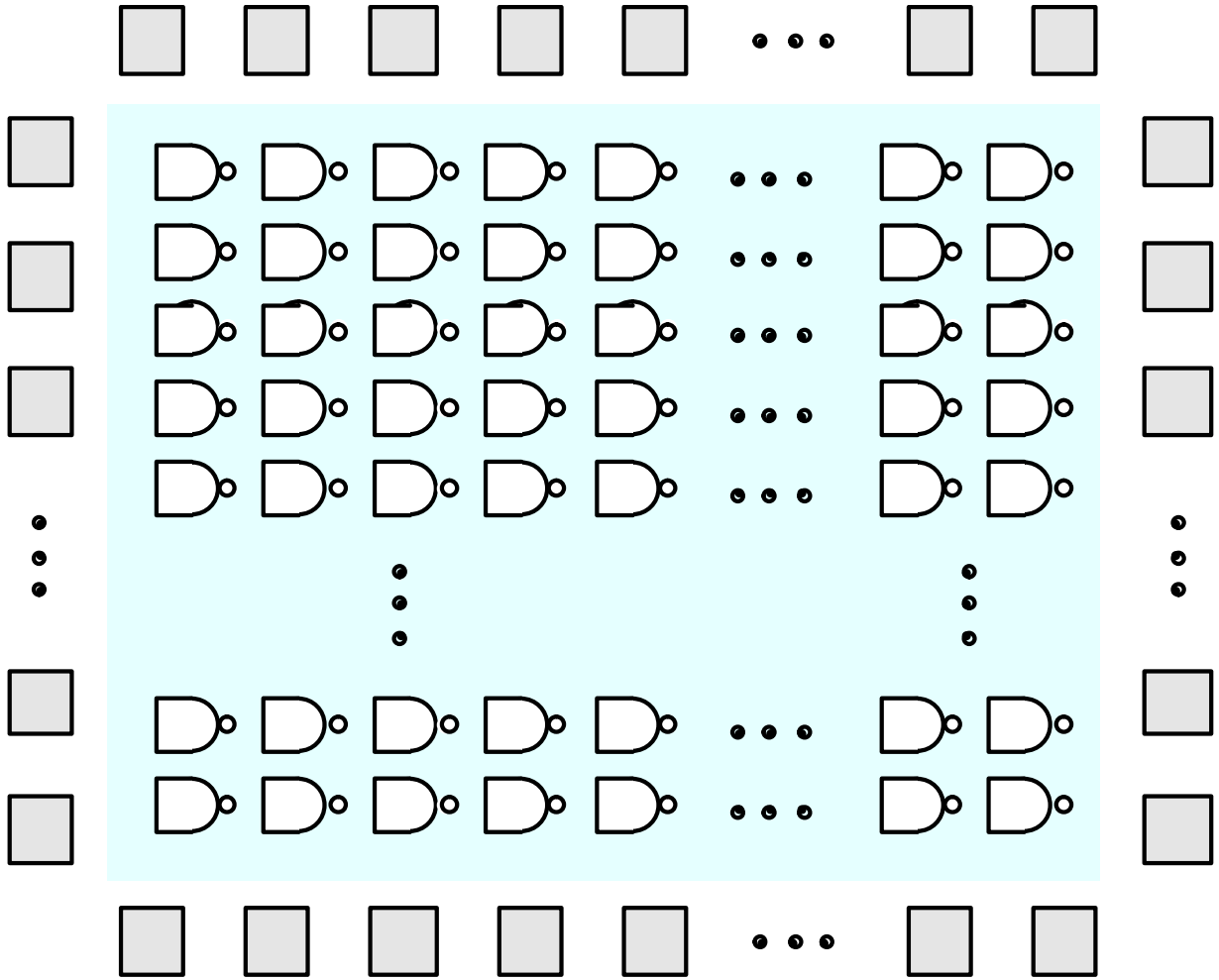


Structure of 7404 chip

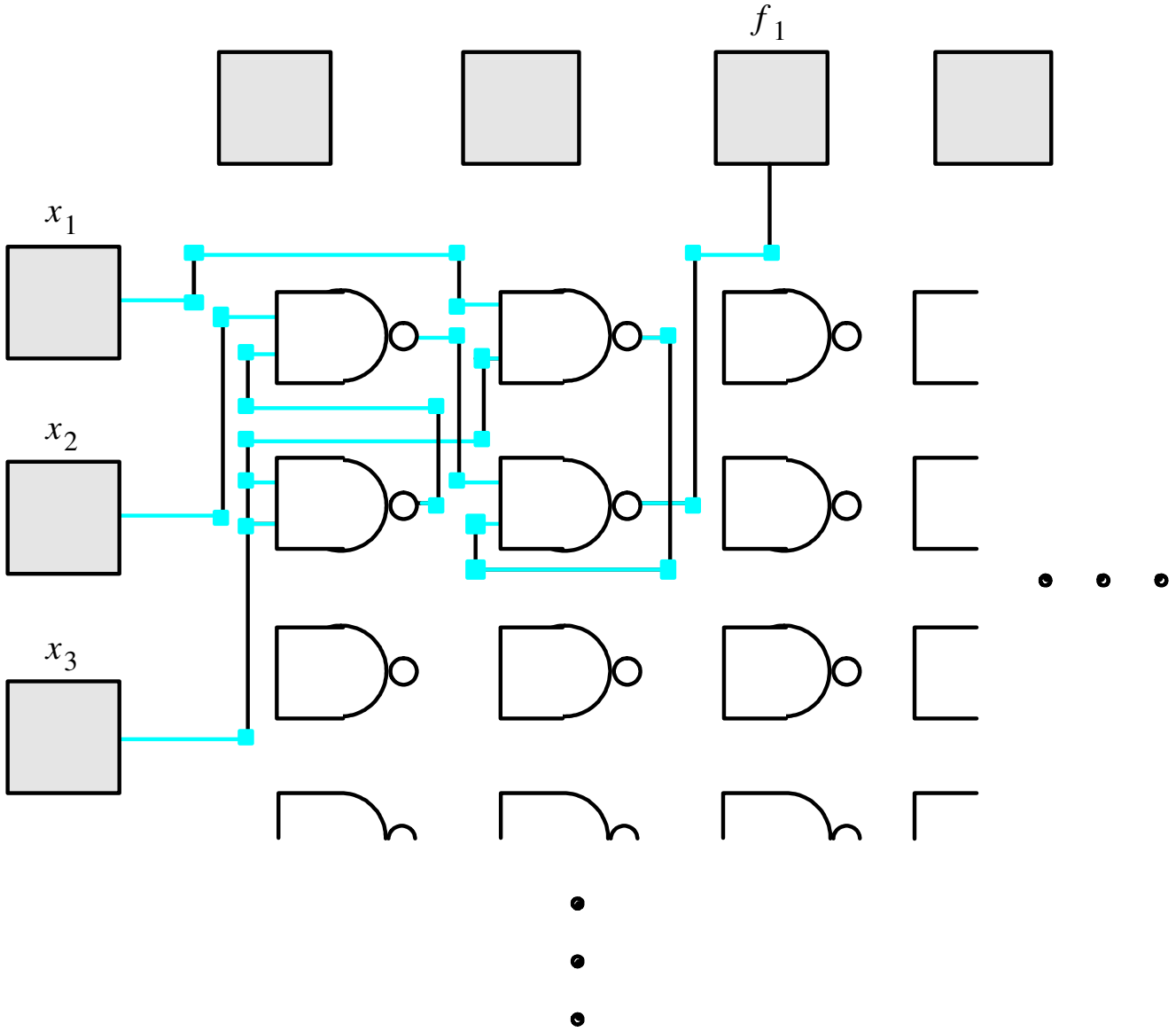


Implementation of $f = x_1x_2 + \bar{x}_2x_3$

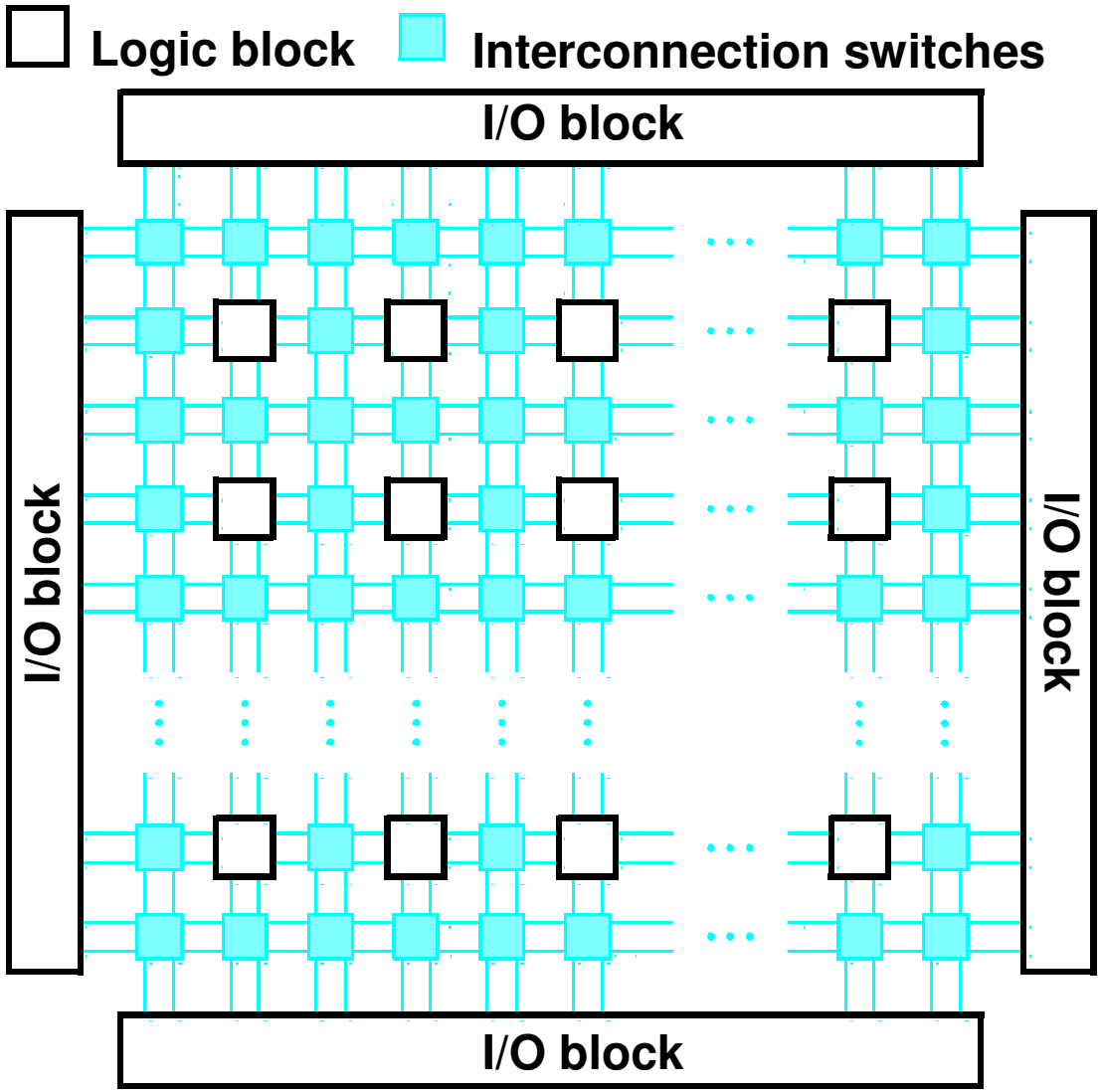
Sea-of-gates Gate Array



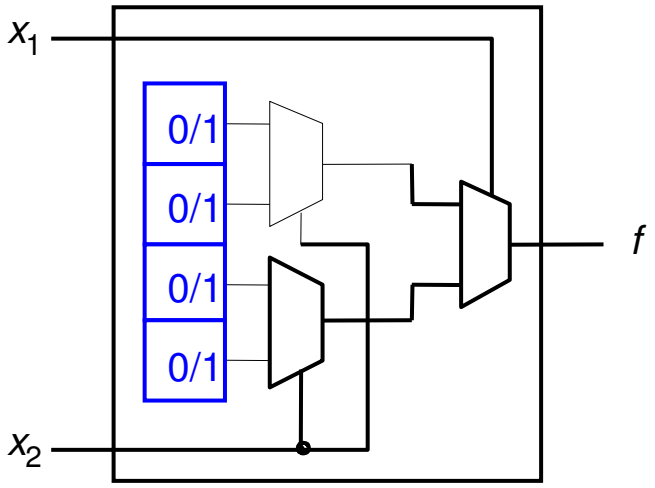
Gate Array



FPGA
Field-Programmable Gate Array



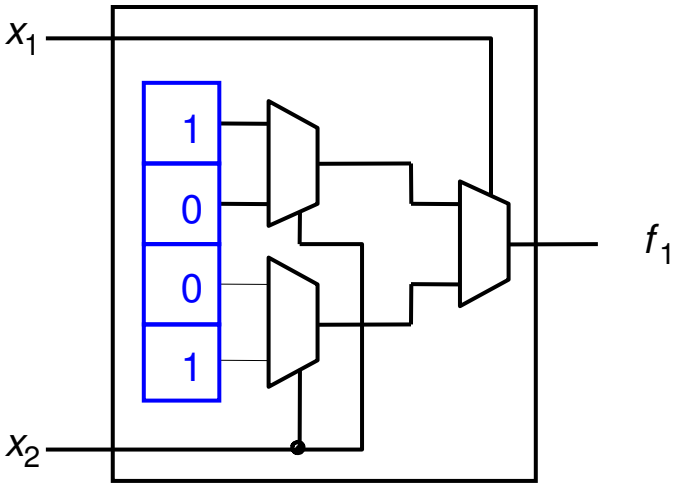
FPGA: Logic Block
LUT – lookup table



(a) Circuit for a two-input LUT

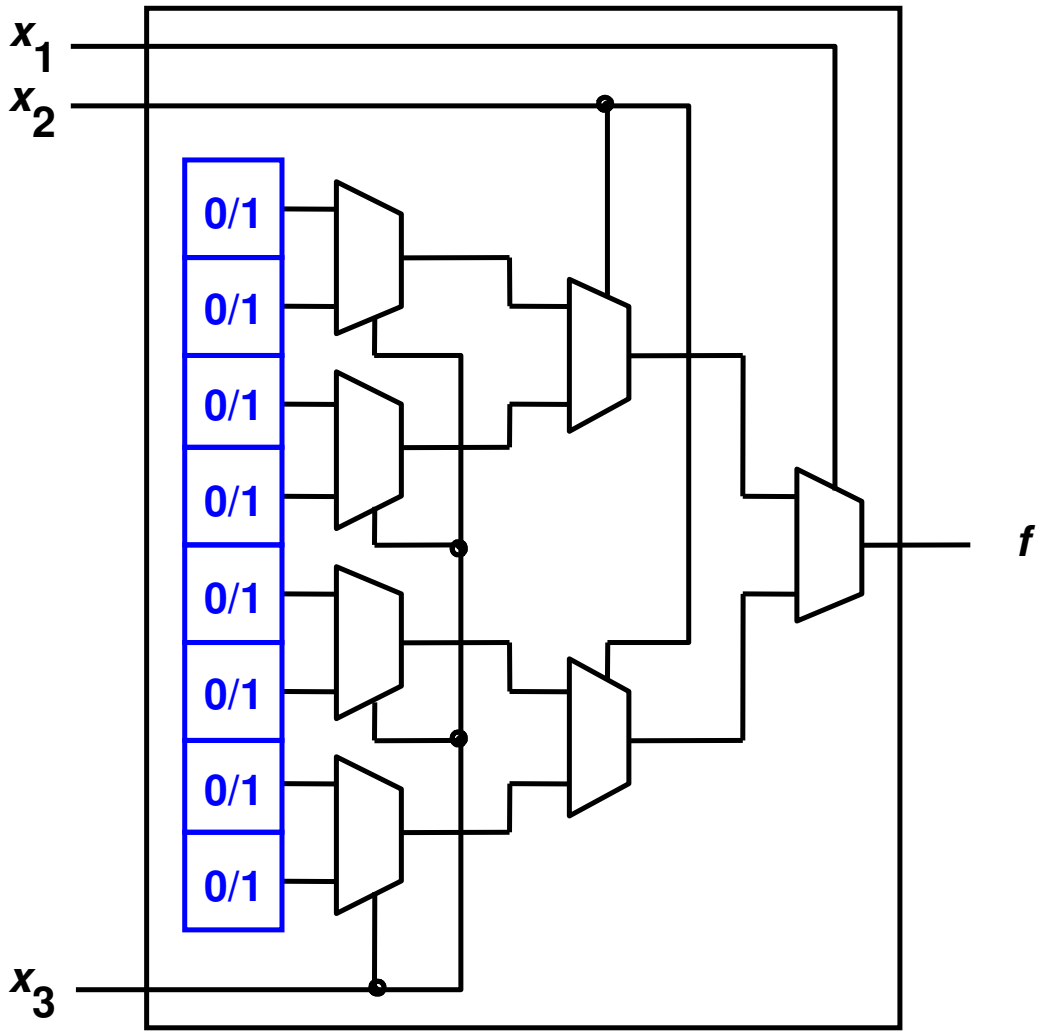
x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

(b) $f_1 = \bar{x}_1 \bar{x}_2 + x_1 x_2$

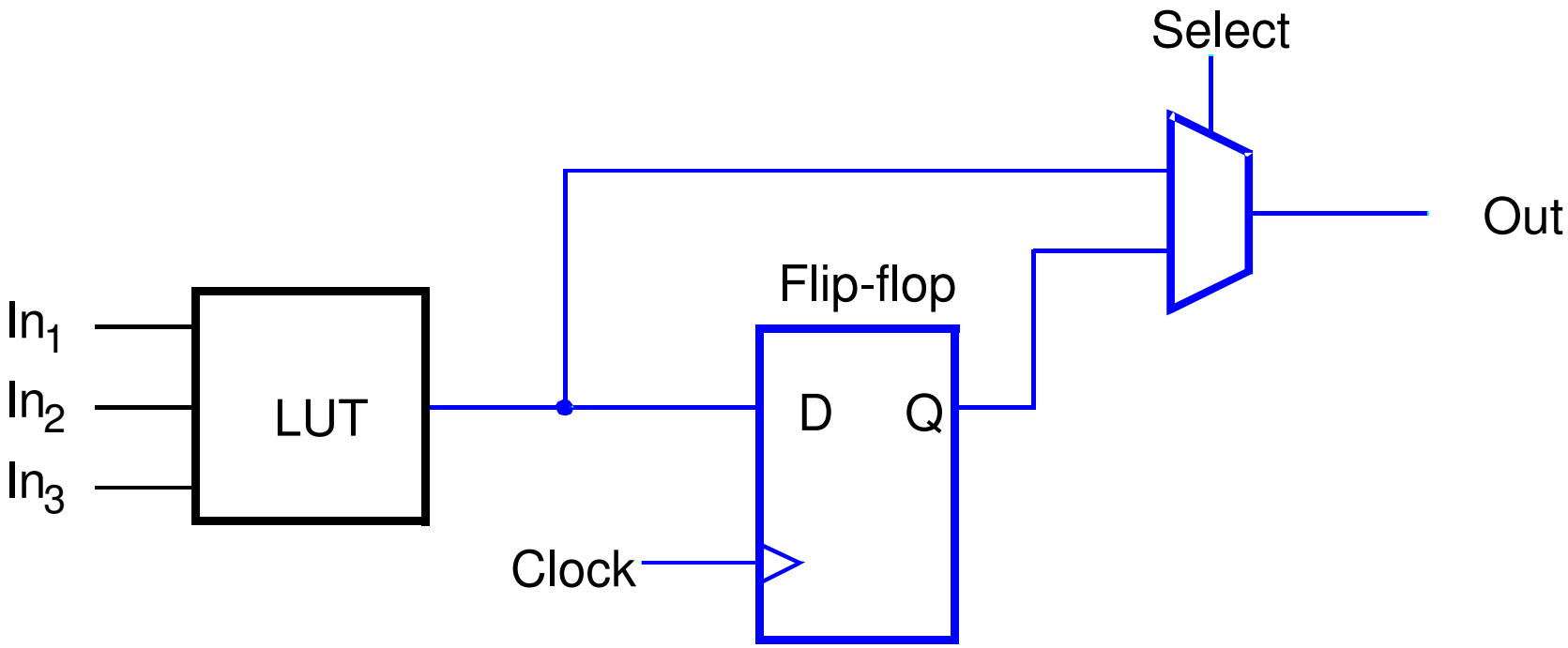


(c) Storage cell contents in the LUT

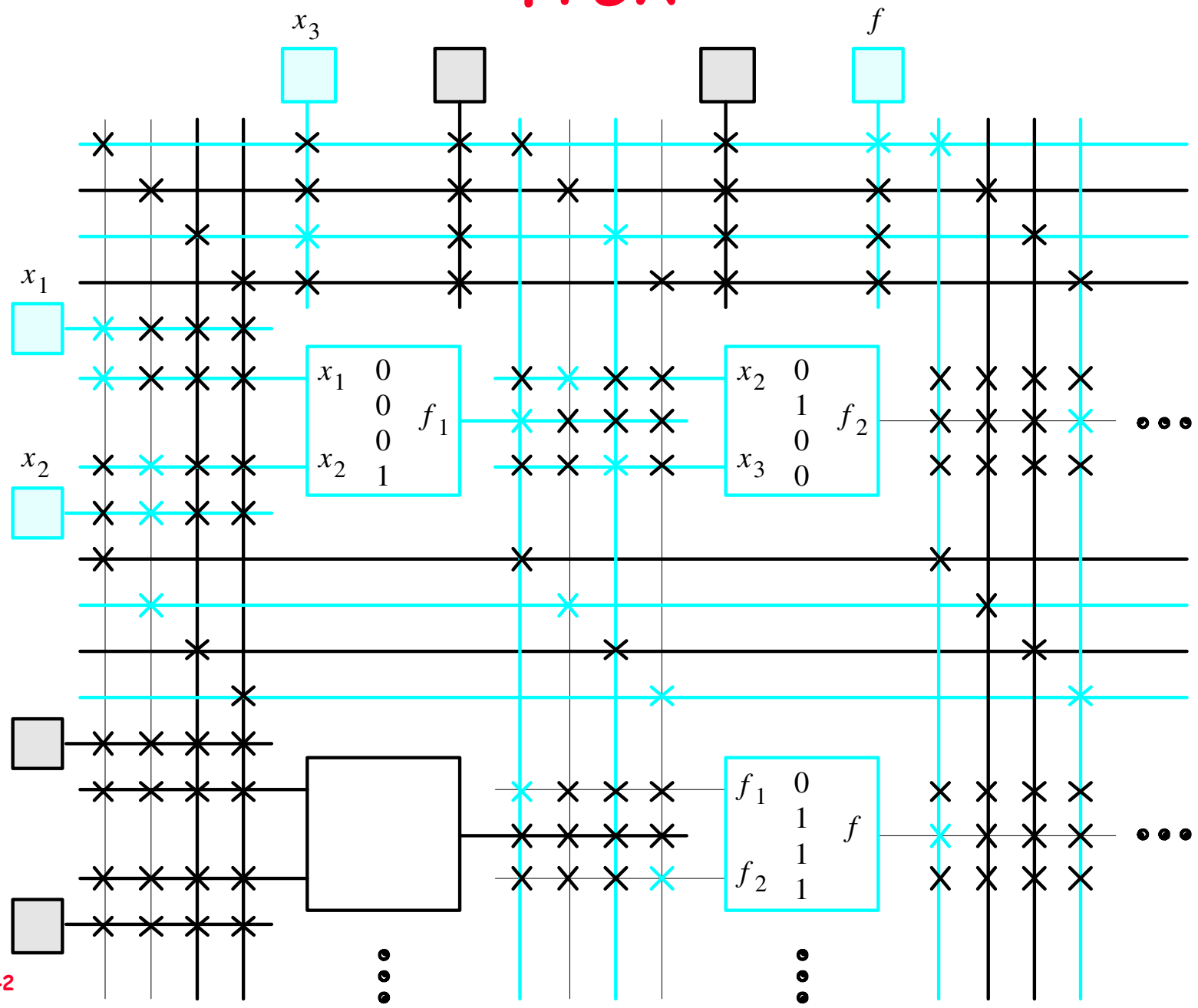
FPGA
LUT



FPGA

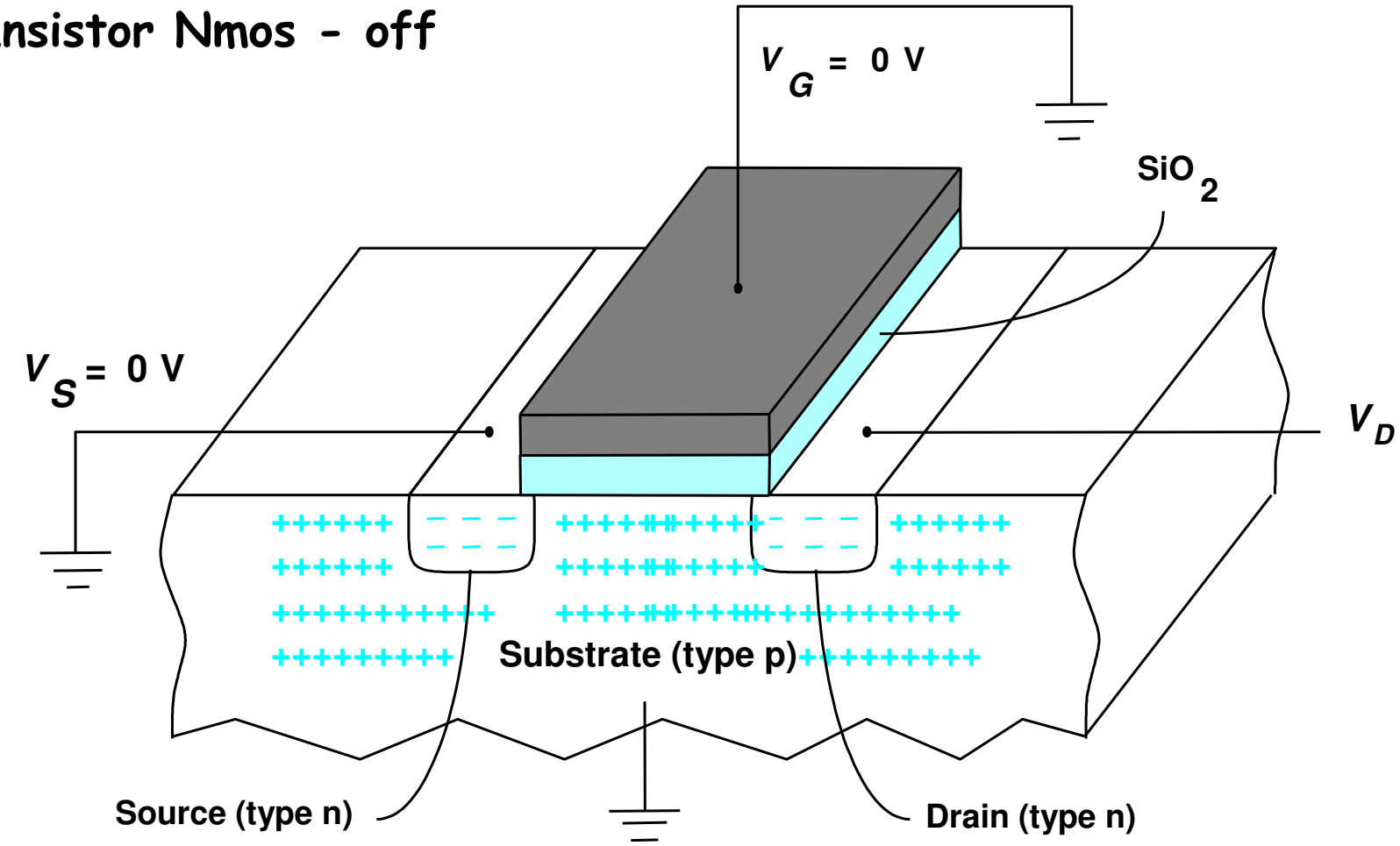


FPGA



CMOS: Fabricação e Comportamento

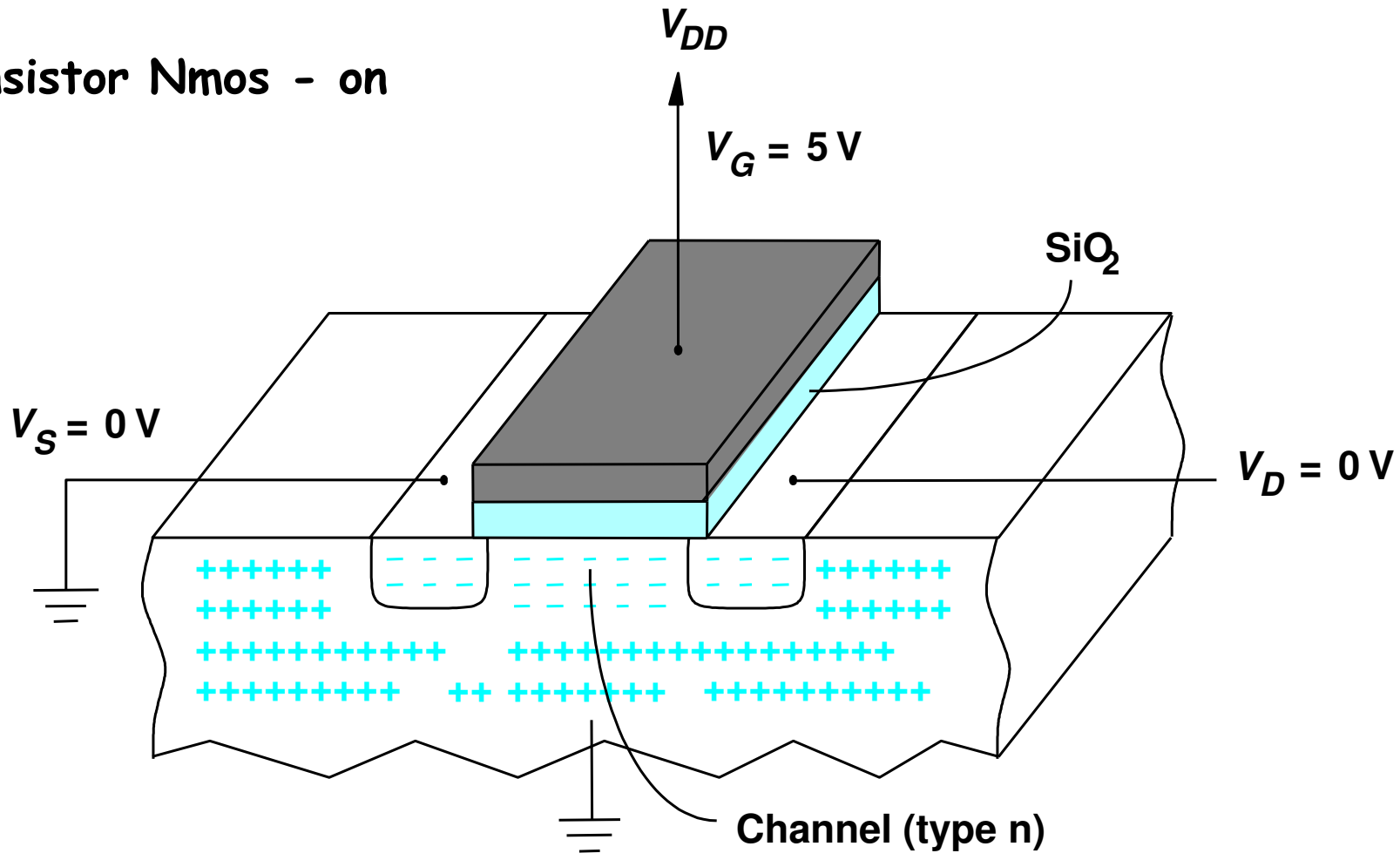
Transistor Nmos - off



When V_{GS} = 0 V, the transistor is off

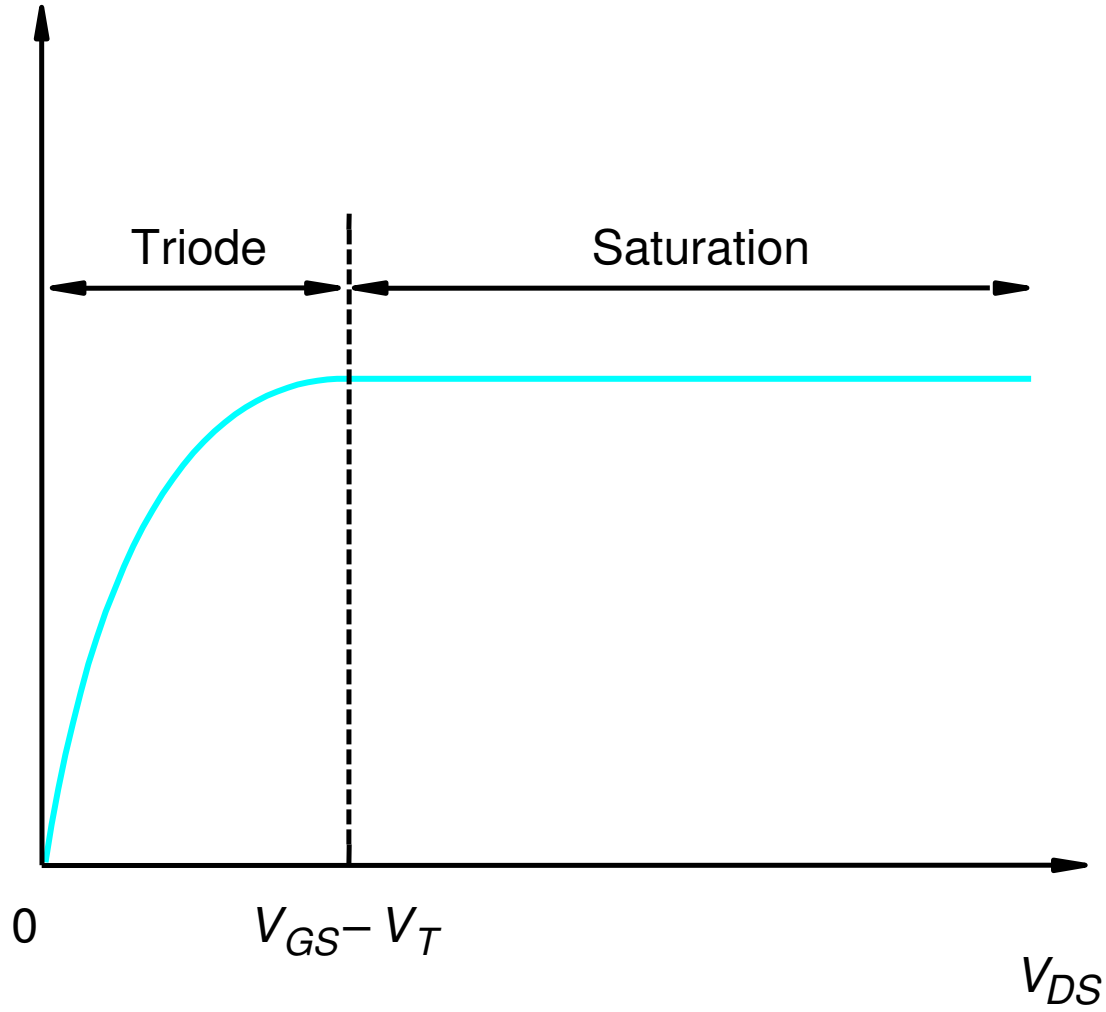
CMOS: Fabricação e Comportamento

Transistor Nmos - on



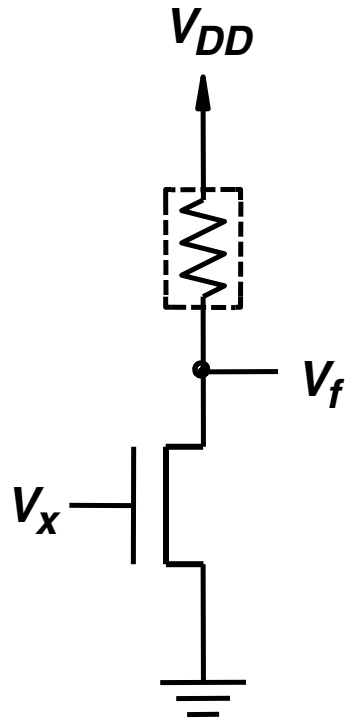
When V_{GS} = 5 V, the transistor is on

Transistor Nmos

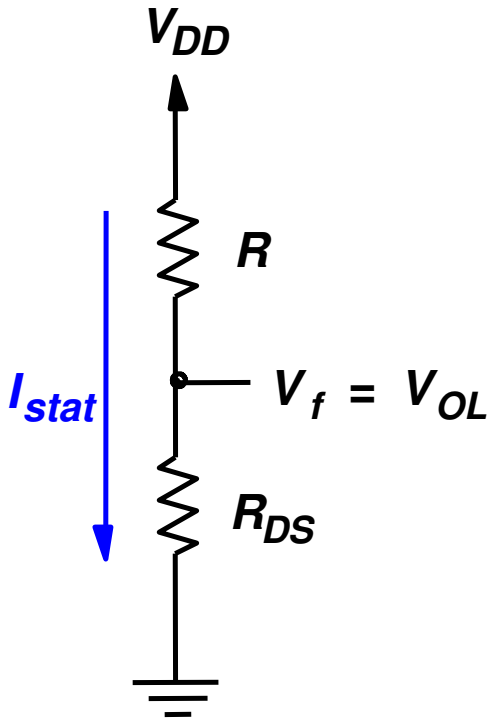


Current-voltage relationship in the NMOS transistor

Tensões em um Not Nmos

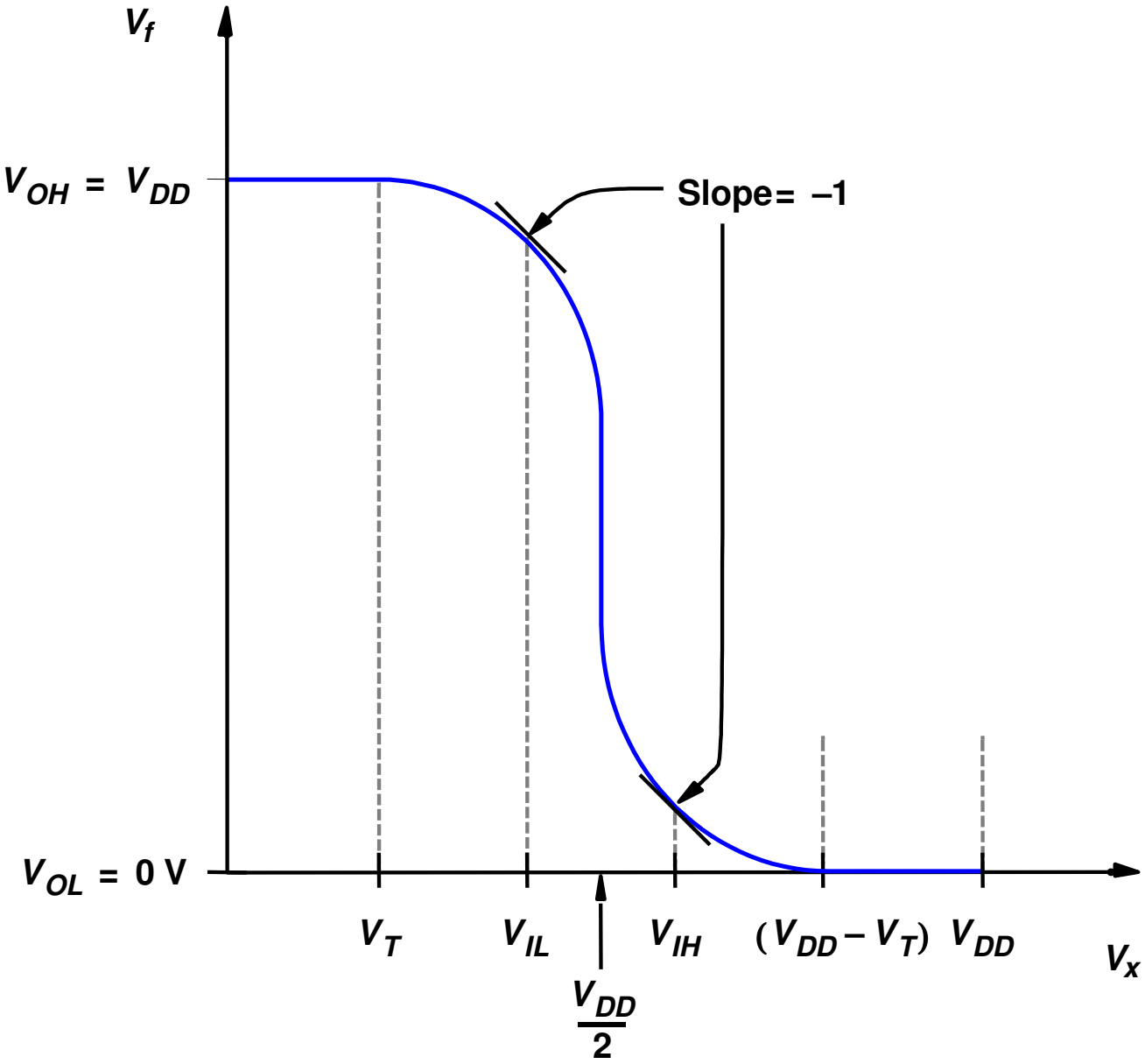


(a) NMOS NOT gate

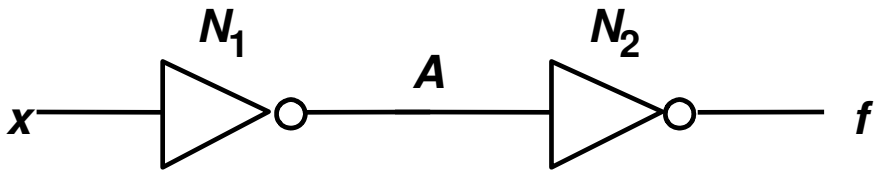


(b) $V_x = 5$ V

Transferência de Voltagem
Not Cmos



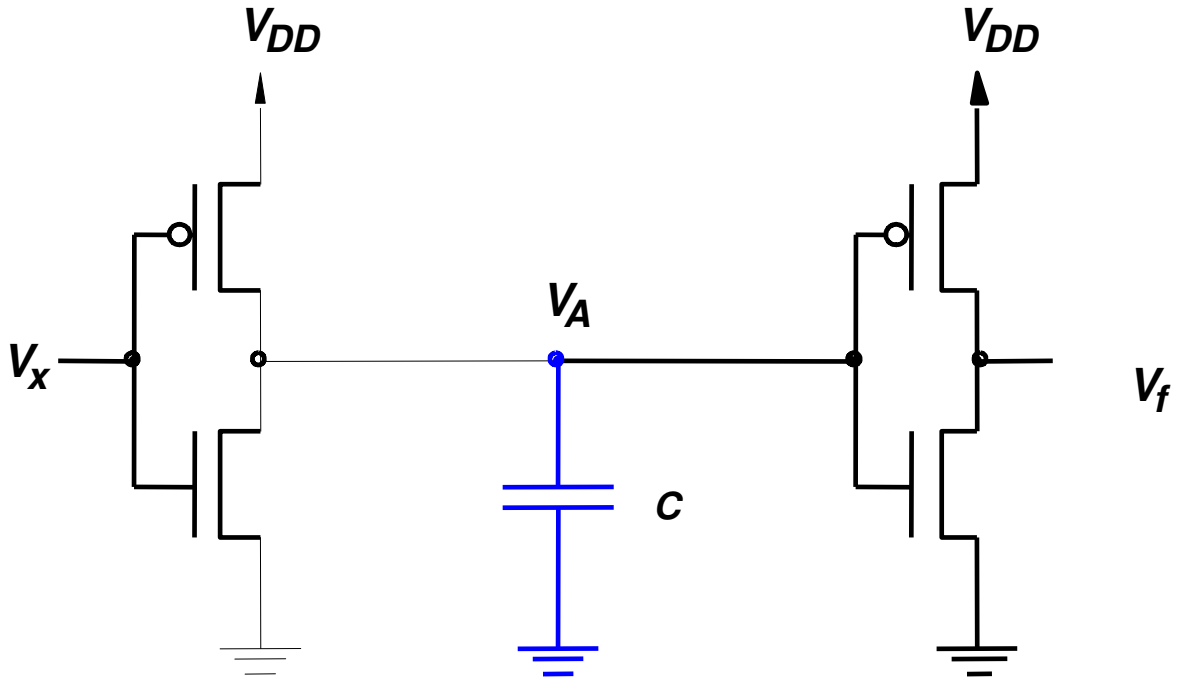
Margem de Ruído e Capacitância



NOT gate driving another NOT gate

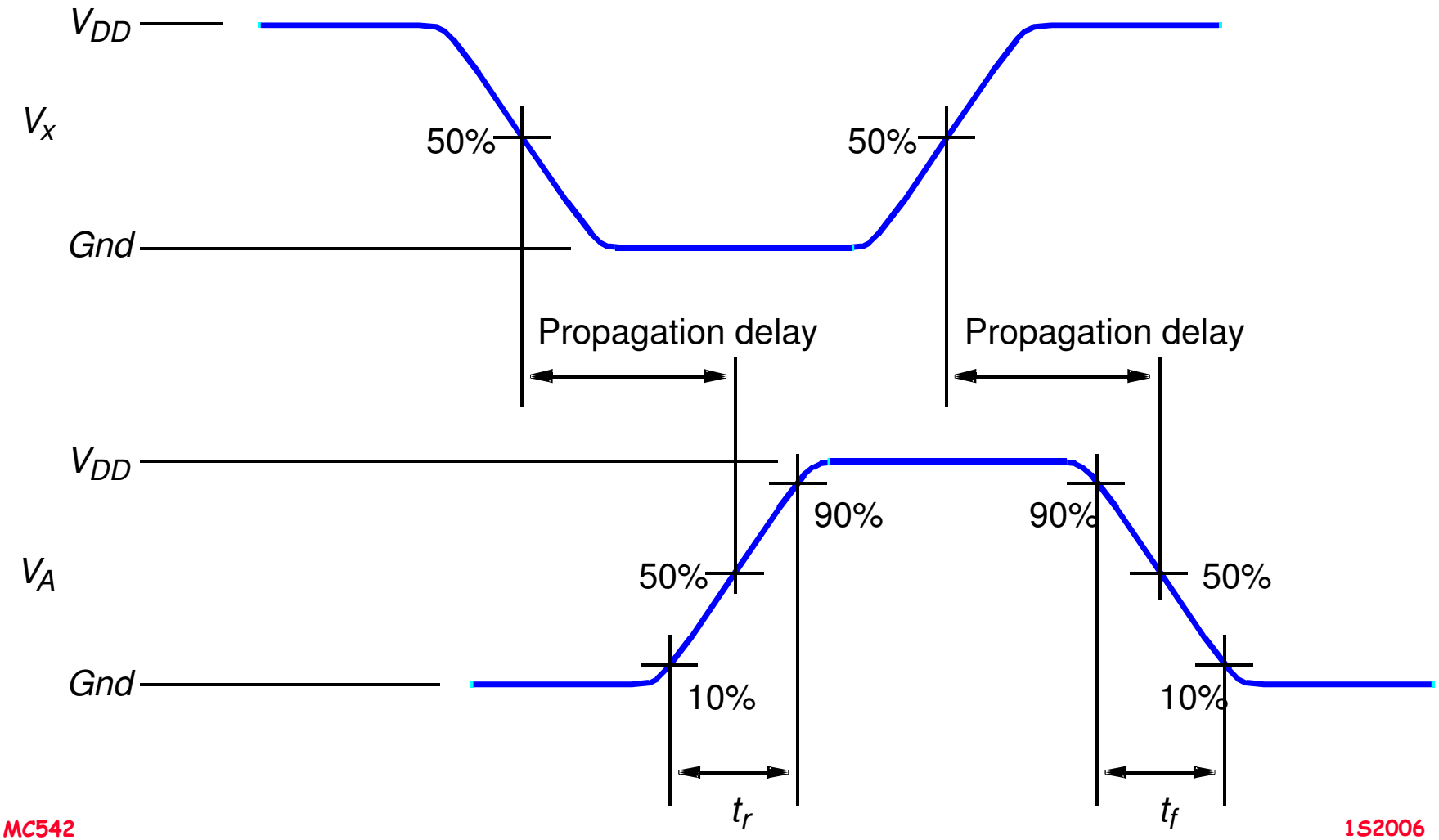
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

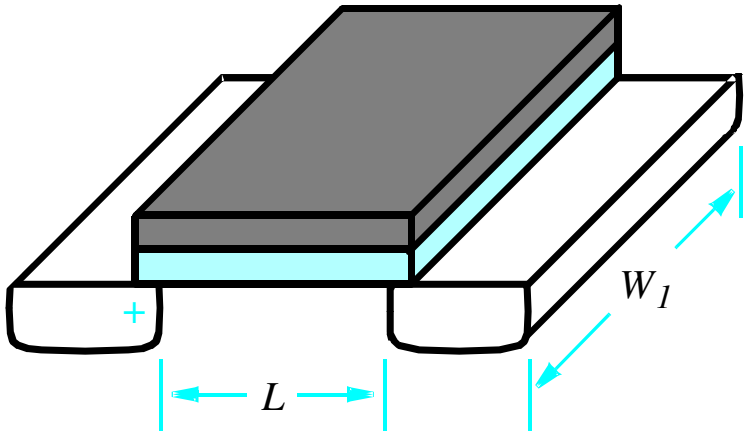


The capacitive load at node A

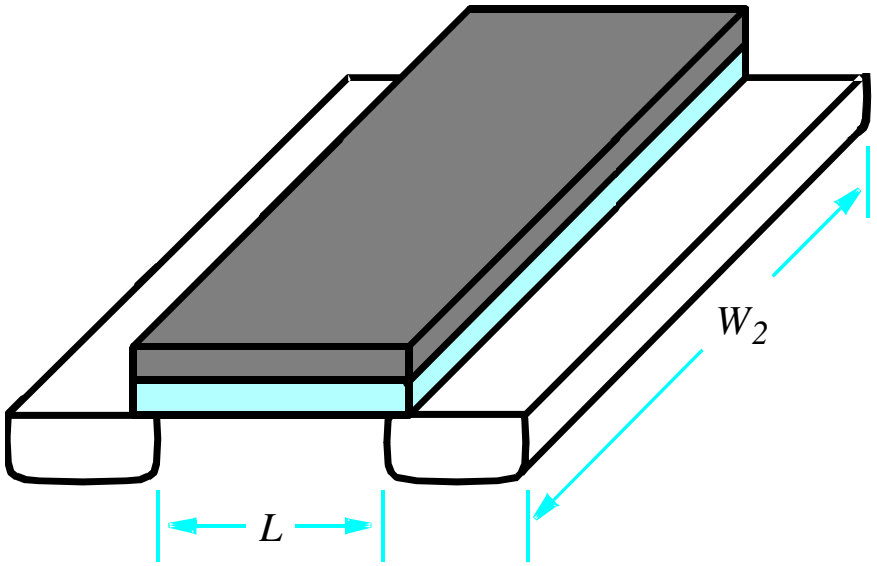
Margem de Ruído e Capacitância



Transistor MOS

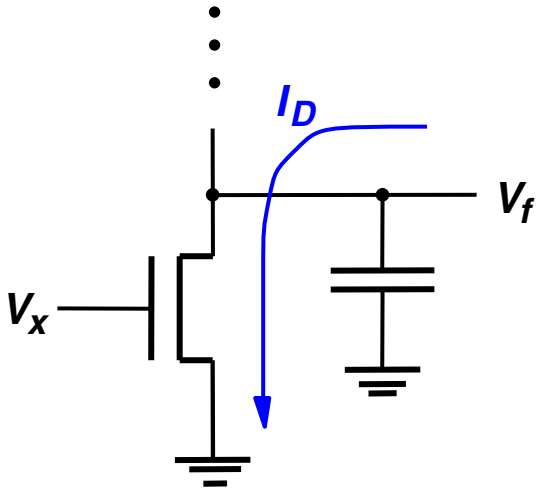


(a) Small transistor

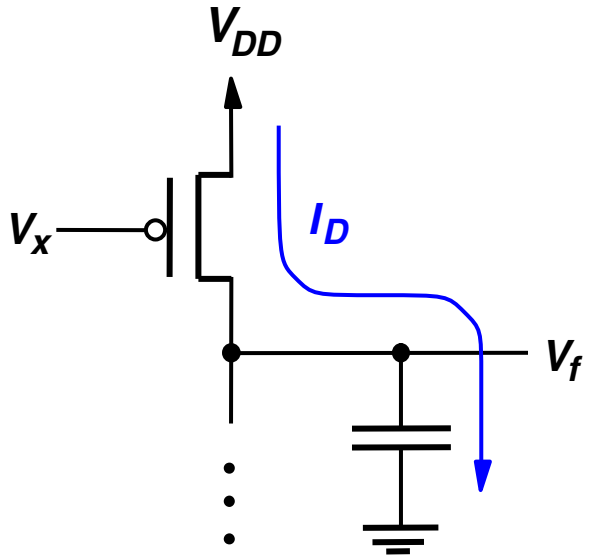


(b) Larger transistor

Consumo de Potência

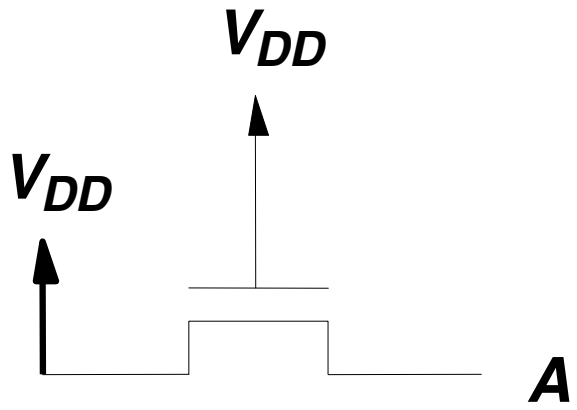


Current flow when input V_x changes from 0 V to 5 V

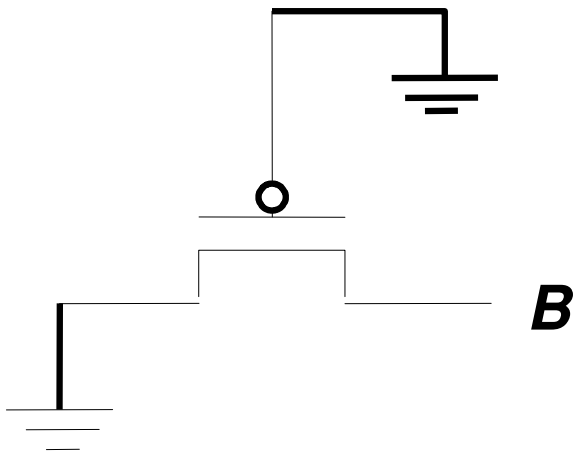


Current flow when input V_x changes from 5 V to 0 V

Passagem de 1s e 0s em MOS

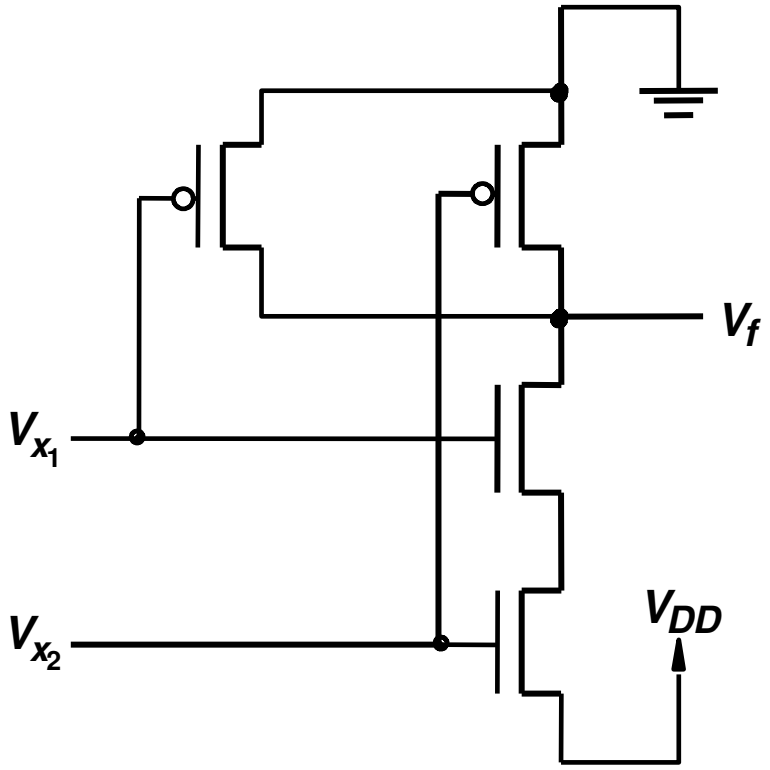


transistor NMOS



transistor PMOS

Implementação "pobre" de um AND CMOS



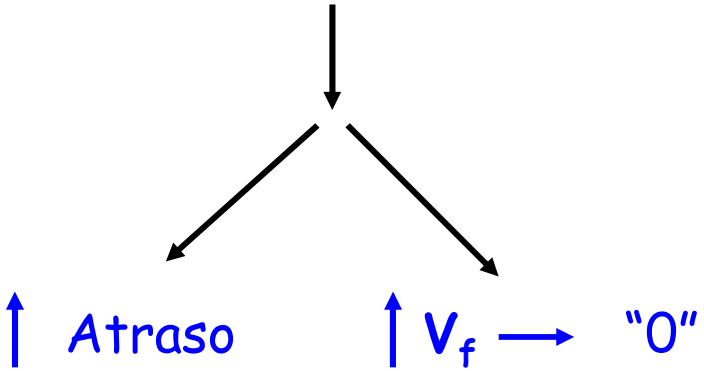
AND gate circuit

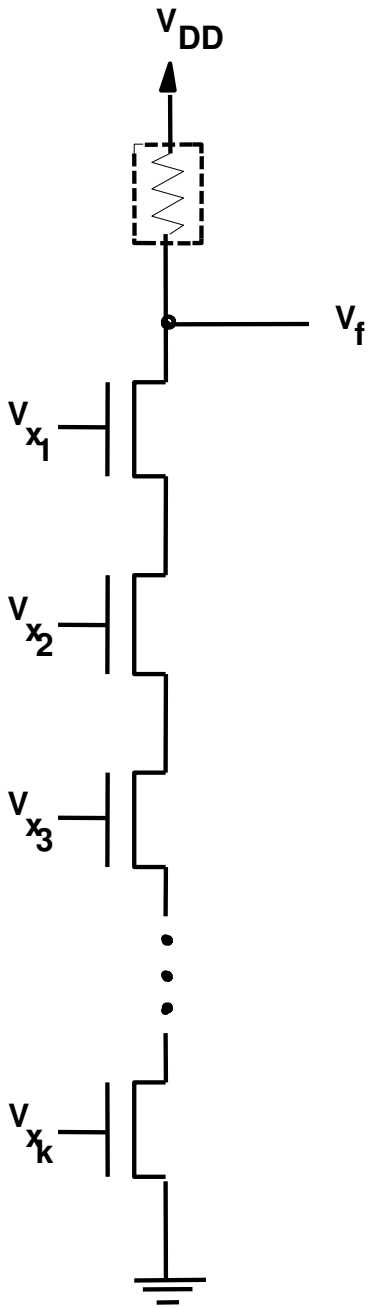
Logic value		Voltage	Logic value
x_1	x_2	V_f	f
0	0	1.5 V	0
0	1	1.5 V	0
1	0	1.5 V	0
1	1	3.5 V	1

Truth table and voltage levels

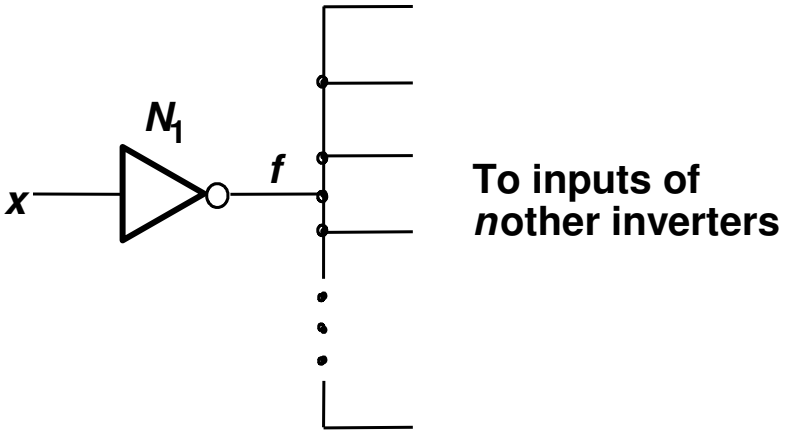
Fan-IN

$R = r_1 + r_2 + \ldots + r_k$

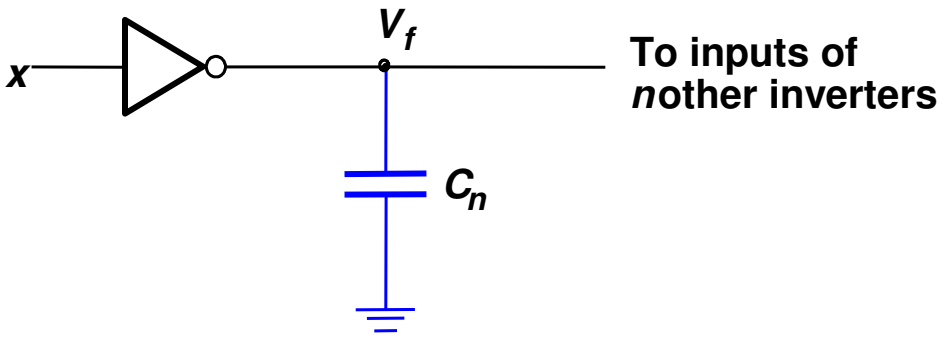




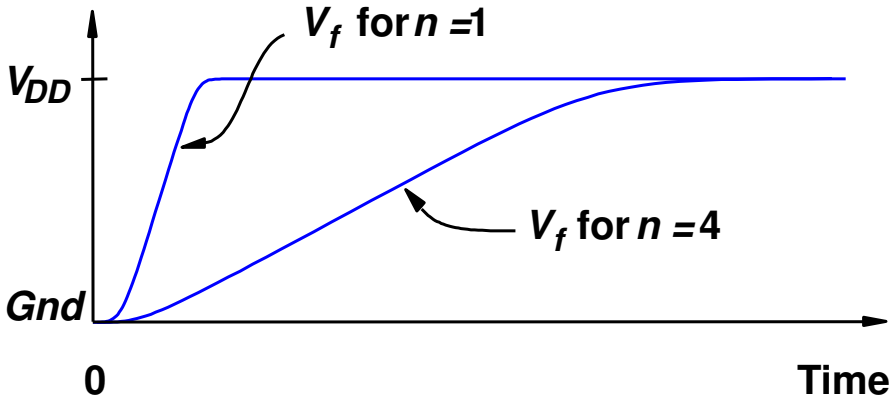
Fan-Out



inverter that drives n other inverters

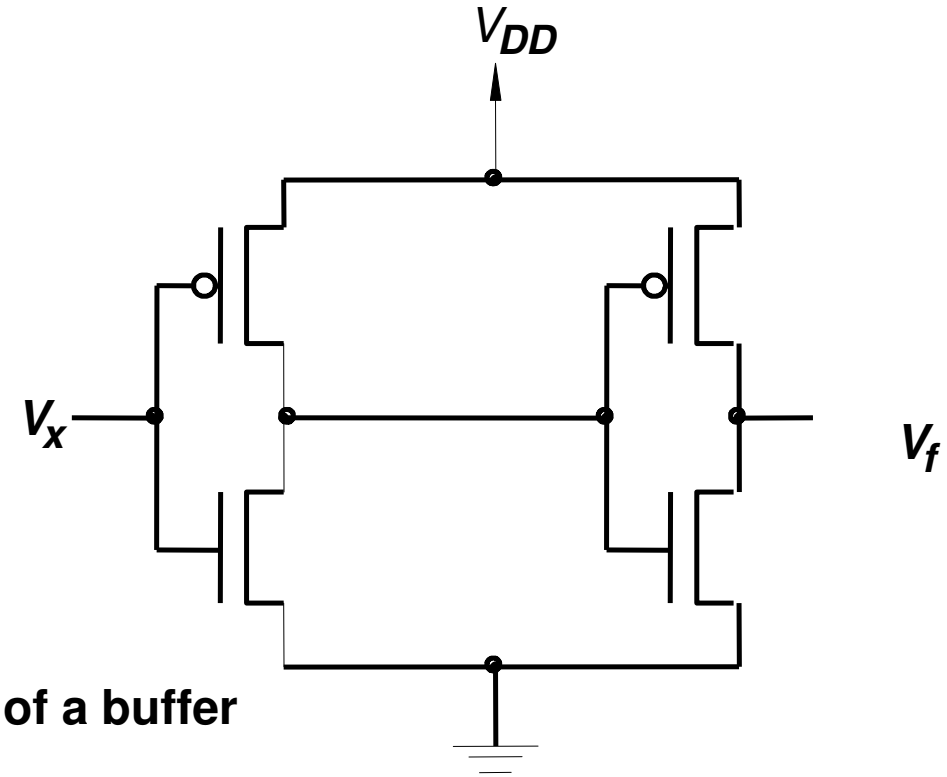


Equivalent circuit for timing purposes

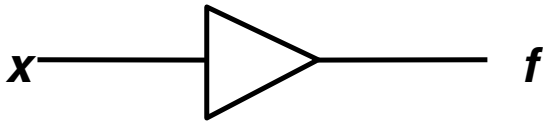


Propagation times for different values of n

Buffer

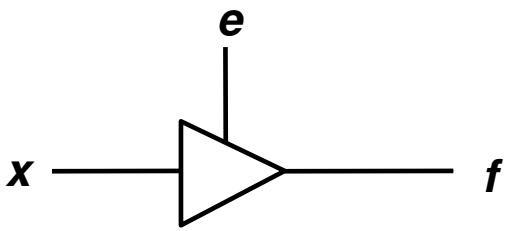


Implementation of a buffer

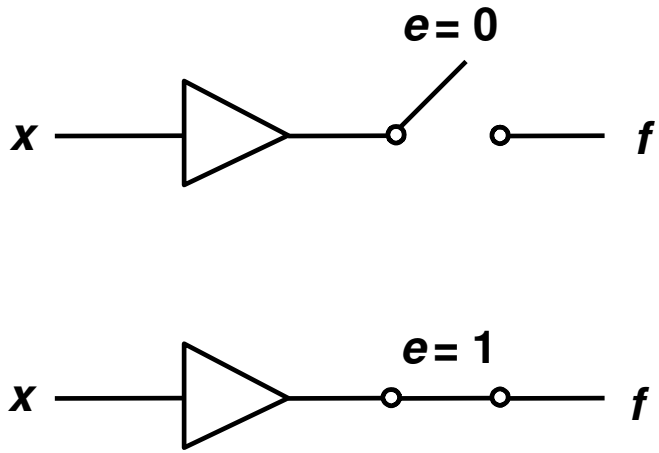


Graphical symbol

Tri-state



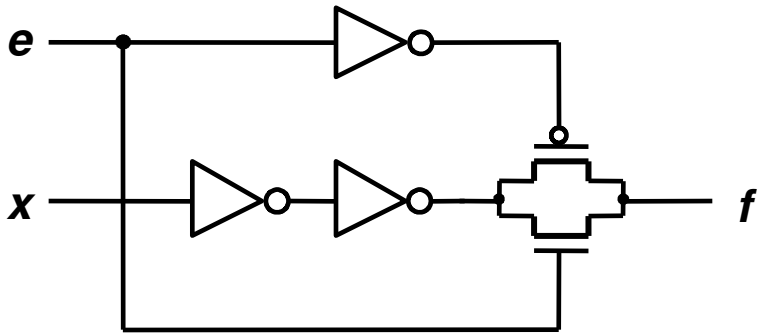
tri-state buffer



Equivalent circuit

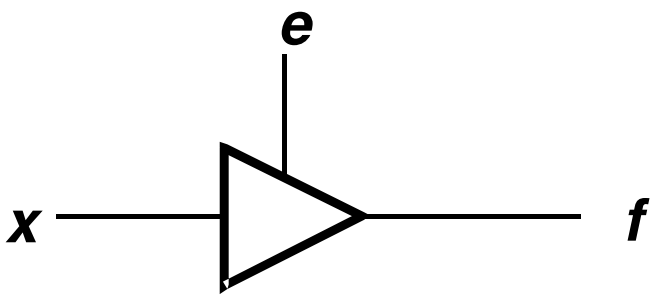
e	x	f
0	0	Z
0	1	Z
1	0	0
1	1	1

Truth table

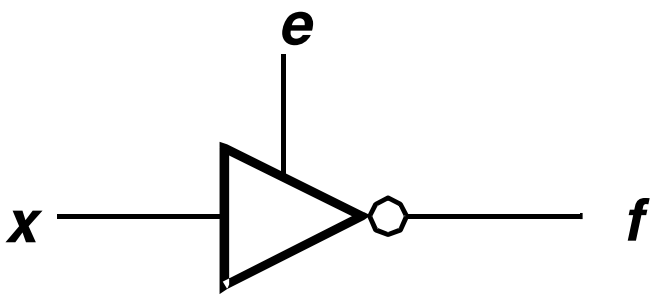


Implementation

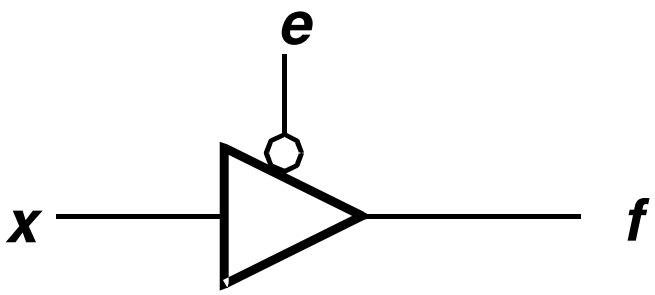
Tri-state



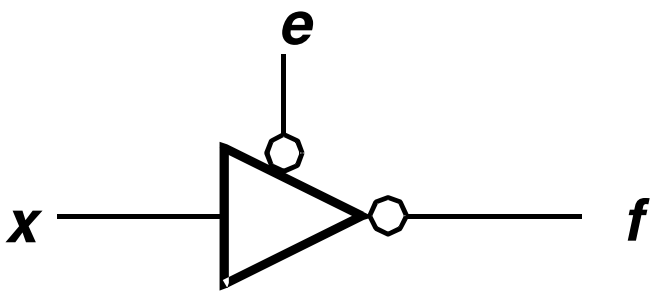
(a)



(b)

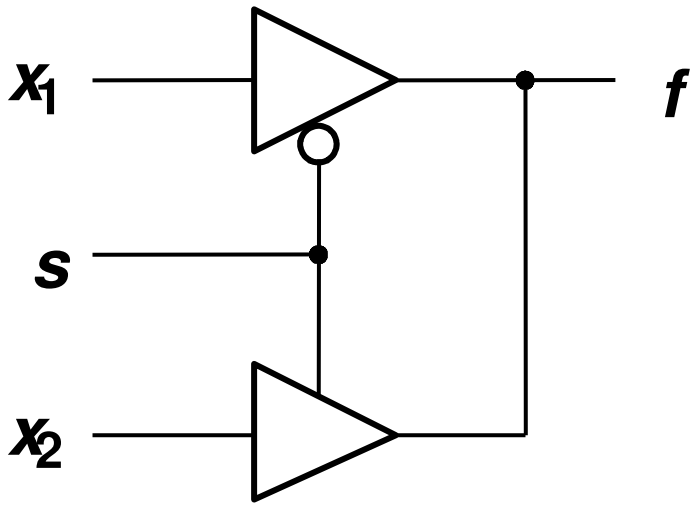


(c)

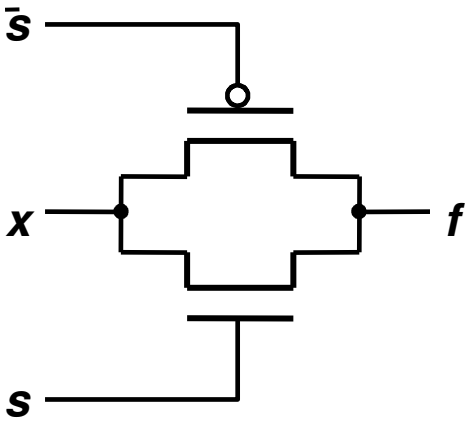


(d)

Uso de tri-state



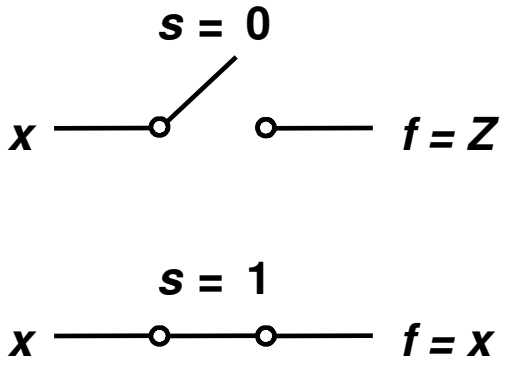
Transmission Gates



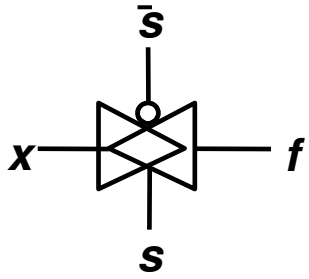
Circuit

s	f
0	Z
1	x

Truth table



Equivalent circuit

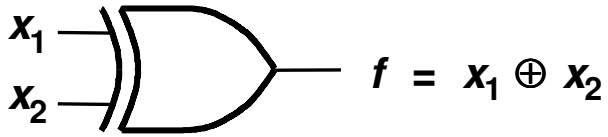


Graphical symbol

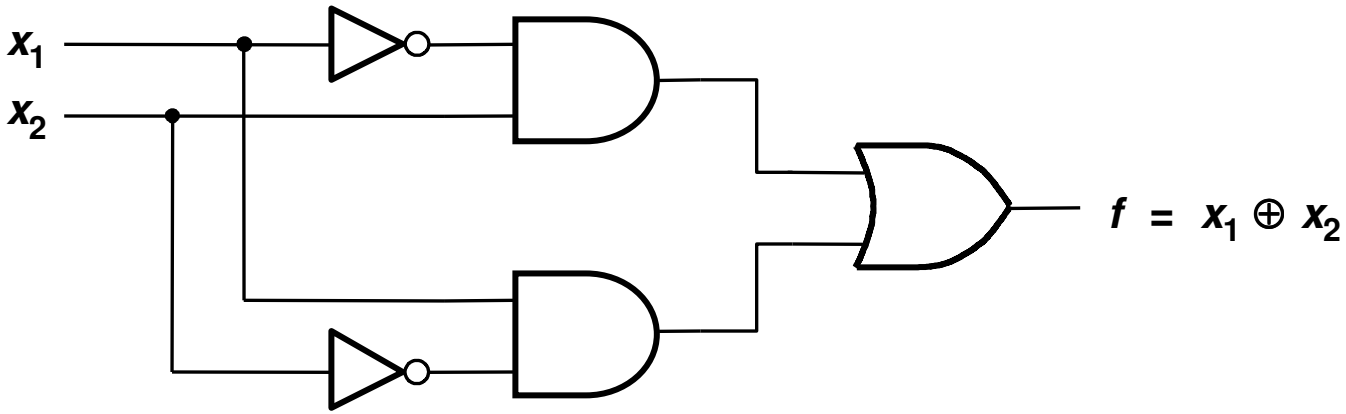
XOR

x_1	x_2	$f = x_1 \oplus x_2$
0	0	0
0	1	1
1	0	1
1	1	0

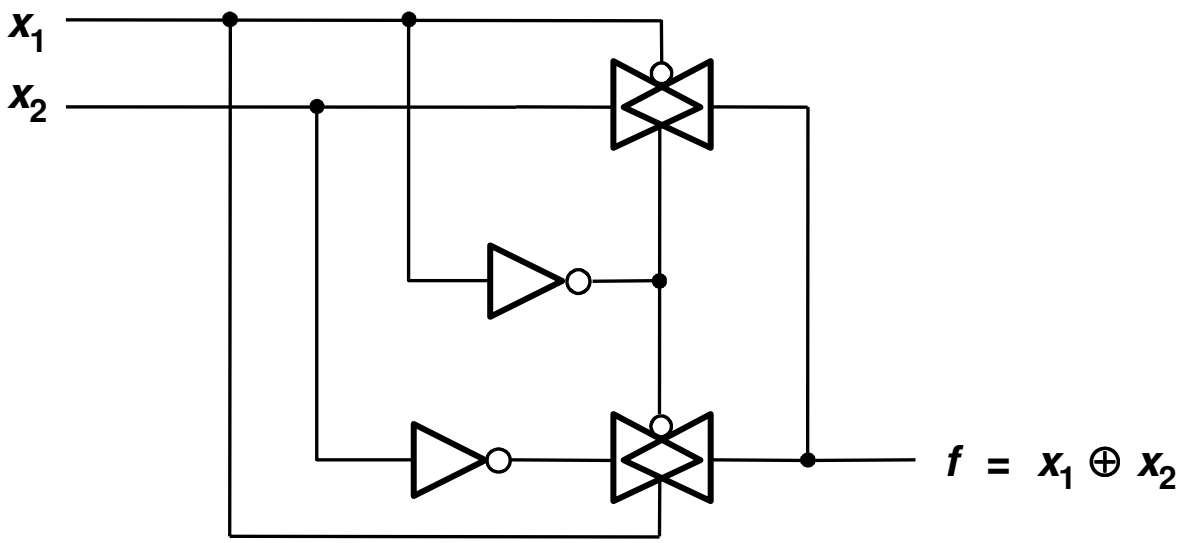
Truth table



Graphical symbol



XOR – Transmission Gate



Mux – Transmission Gate