Parallel Computer Architecture: A Hardware/Software Approach

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ERRATA FOR FIRST PRINTING *

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	Page	Error
1.	60	Equation 1.4, change $\frac{T_0}{B}$ to T_0B
2.	73	Exercise 1.9, replace the last three sentences, the first beginning "Compare this" with "Graph the average message rate as a function of m for various values of $T = 100$ ns, 200 ns, 400ns, 800 ns. What is the asymptote?"
3.	73	Exercise 1.15, replace the last two sentences, the first beginning "If data undergoes" with "Assume that before transmitting a message, the data must be copied into a buffer. The basic message time is as in Exercise 1.14, but the copy is performed at a cost of 5 cycles per 32-bit word on a 100-MHz machine. Give an equation for the expected user-level message time. How does the cost of a copy compare with a typical fixed cost of entering the operating system?"
4.	74	Exercise 1.16, line 6, delete "50% of"
5.	74	Exercise 1.17, lines 1-2, delete "leaving 50% headroom on the bus to make the calculation reasonable"
6.	94	Figure 2.7, line 14, delete "diff = 0,"
7.	104	Figure 2.13, line 15, change "/*outer loop over all diagonal elements*/" to "/*loop until converge*/"
8.	106	Line 4, change "cell_lock" to "diff_lock"
9.	107	Figure 2.14, change "b: flag" to "b: flag = 1;" and delete "=1;" after "a: while (flag is 0) do nothing;"
10.	114	Figure 2.17, align lines 25k and 25m with "if" in 25c
11.	133	Figure 3.4, in both cases, change $\frac{n}{p}$ to $\frac{n}{\sqrt{p}}$
12.	166	Figure 3.15, swap placement of graphs a and b
13.	166	Figure 3.15, line 2 of the figure caption text, change "1,030 \times 1,030" to "1,026 \times 1,026"

^{*} All line numbers refer to running text and do not include tables, figures, or code samples

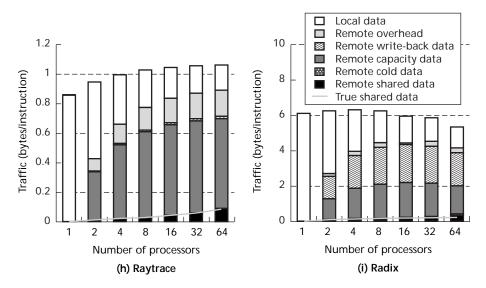
14. 174 Figure 3.19, change "costzone" to "costzones" 15. 179 Figure 3.21, swap placement of graphs a and b 16. 255 *In the line for the Radix*, make the following changes: "256-K integers" "256-K points" to "84.62" "14.02" to "14.19" "5.27" to "7.81" "2.90" to "2.37" "6.38" to "3.61" "1.34" to "2.18" "0.81" to 17. 308 In the Radix section, replace the data with the following: NP 0 0 0.004746 3.524705 11.41111 ı 0.130988 0 0 1.108079 4.57868 Ε 0.000759 0.002848 0.080301 0 0.00019 S 0.029804 1.120988 0 178.1932 0.817818 M 0.044232 11.53127 0 4.03157 802.282 18. In the Raytrace section, under "S", change "0.15486" to "1.5486" 309 19. 309 In the sentence at the bottom, insert "(except for Multiprog, which is for 8 processors)" after "The data assumes 16 processors" 20. 310 Line 16, delete "or per FLOP" 21. 310 Line 8, delete reference to footnote 5 22. 310 Paragraph after "Answer", move inline with "Answer" and insert reference to footnote 5 after the last sentence 23. 310 In the footnote, lines 4-5, replace "the bus traffic data that we will compute using these numbers" with "how we compute data traffic, but it means that instruction traffic is computed differently" 313 Line 11, change "depend" to "depends" 24. 25. 313 Lines 15-16, delete "64 KB" 26. 313 Line 17, after the sentence ending "cache hierarchy," insert the following sentence, "We use 64-KB caches here, which fit all but the largest working set for these problem sizes." 27. 314 *In the Radix section*, replace the data with the following: NΡ 0 0 9.440787 2.557865 27.36084 ı 4.354862 0 0.00057 0.157565 1.499903 Ε 140.9295 8.148377 0.001329 0.012339 0.126621 S 0.484464 3.825407 0.481427 0 102.4144 M 23.03084 5.629429 0 2.069604 717.1426

Line 18, change "(case 11)" to "(case 9)"

28.

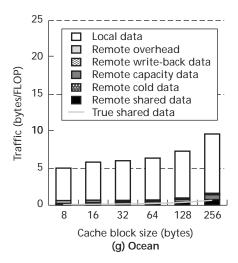
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- 29. Lines 9-10, replace "down from $O(p^2)$ to O(p) per lock acquisition, but still increases with the number of processors" with "and there are no read-modify-write bus transactions, but traffic still increases linearly with the number of processors (i.e., O(p) bus transactions per lock acquisition)"
- 30. 396 Line 1, change ">=" with " \geq "
- 31. 396 Line 4, change "=<" to " \leq "
- 32. Line 26, after the sentence ending "flat directory protocol", add the following two sentences, "Two changes are made from the experiments in Chapter 5. Since Radix sorting would exhibit a lot of false sharing at larger processor counts (our default here is 32 rather than 16 processors), we use a problem size of 1M rather than 256K keys. And we use 8-KB rather than 64-KB caches in all our smaller cache size experiments, to see the effect of even fewer working sets fitting in the cache."
- 33. Figure 8.10, line 2 of the figure caption text, change "64 KB" to "8 KB"
- 34. 581 Figure 8.10, replace graphs h and i with the following:



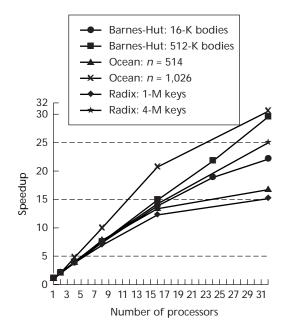
- 35. Figure 8.11, line 1 of the figure caption text, insert "Data are shown for 32-processor executions." before the sentence beginning, "The overhead..."
- 36. Figure 8.11, line 2 of the figure caption text, change "64-KB" to "8-KB"

37. *Figure 8.11*, replace graph g with the following:

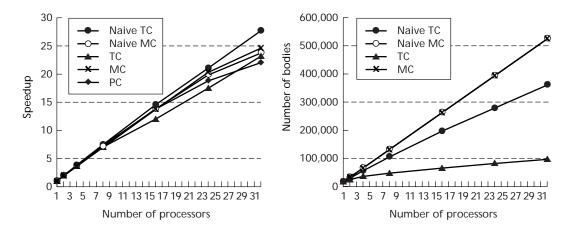


38. Table 8.1, 3rd and 4th columns, rows 4-6, make the following changes:

- 39. Line 9, change "most notably" to "to an extent"
- 40. Line 16, change "doesn't alleviate the situation" to "only alleviates false sharing"
- 41. *Figure 8.22*, replace the graph on the left with the following:



42. *Figure 8.23*, replace with the following:



(To show the Naïve MC line more clearly, its marker has been changed to an unfilled circle.)

- 43. Lines 37-38, delete "and in fact the queuing lock incurs contention on its compare&swap operations (implemented with LL SC) and scales worse than the array lock."
- 44. *Figure 8.34*, replace graph a with the following:

