



# MC 602

## Circuitos Lógicos e Organização de Computadores

IC/Unicamp

Prof Mario Côrtes

### Capítulo 3

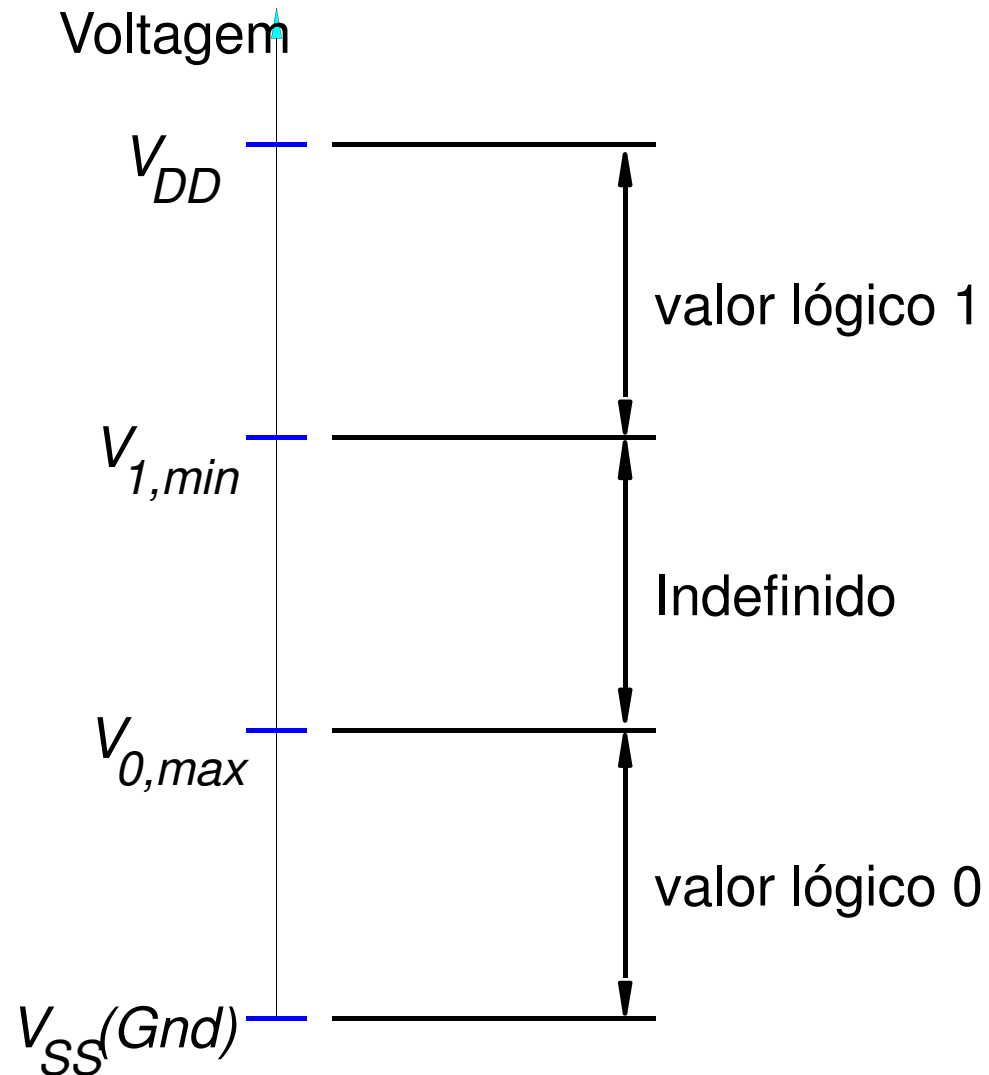
## Tecnologia de Implementação

# Tópicos

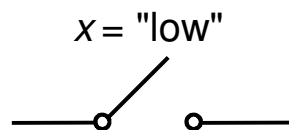
- Transistores
- Portas NMOS
- Portas CMOS
- Lógica e positiva negativa
- Circuitos comerciais
- Atraso
- Margem de ruído
- Potência
- Buffer tri-state

# Valores lógicos e níveis de tensão

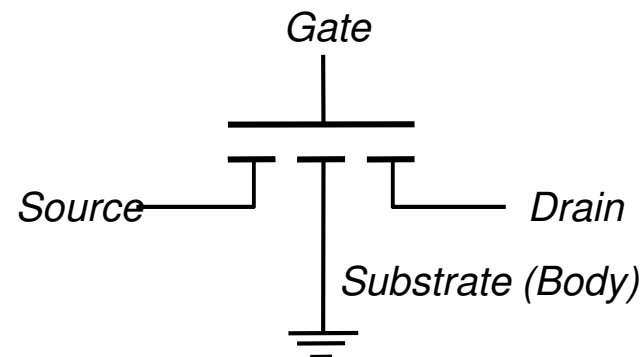
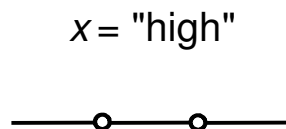
- Vdd típico
  - 5V
  - pode baixar até 1-2V
- Vss típico
  - gnd = 0 V



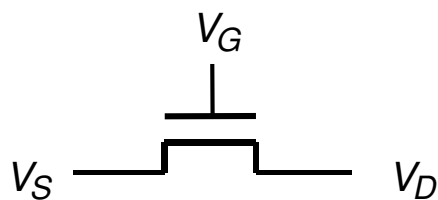
# Transistor NMOS como chave



(a) chave simples controlada por entrada  $x$



(b) transistor NMOS

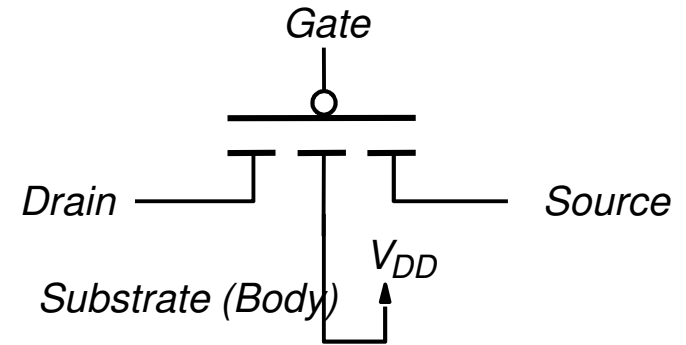


(c) símbolo simplificado para o transistor NMOS

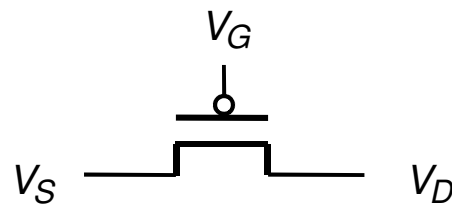
# Transistor PMOS como chave



(a) chave com comportamento oposto ao slide anterior



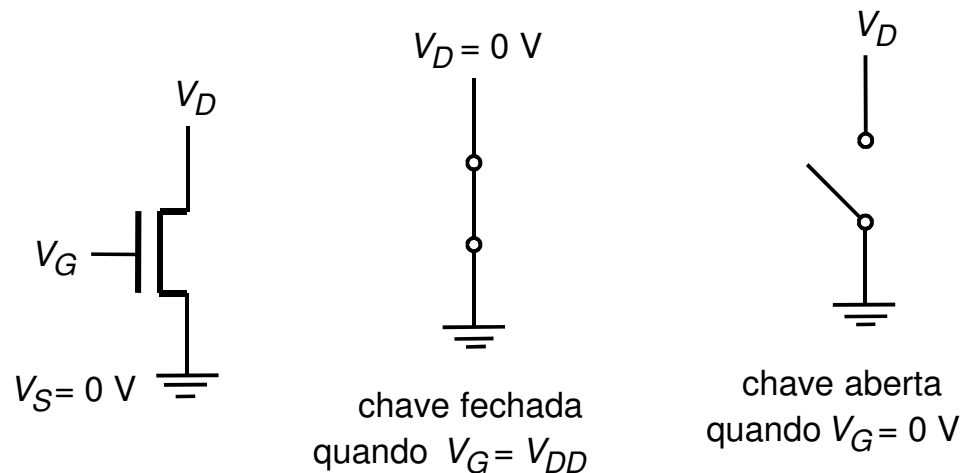
(b) transistor PMOS



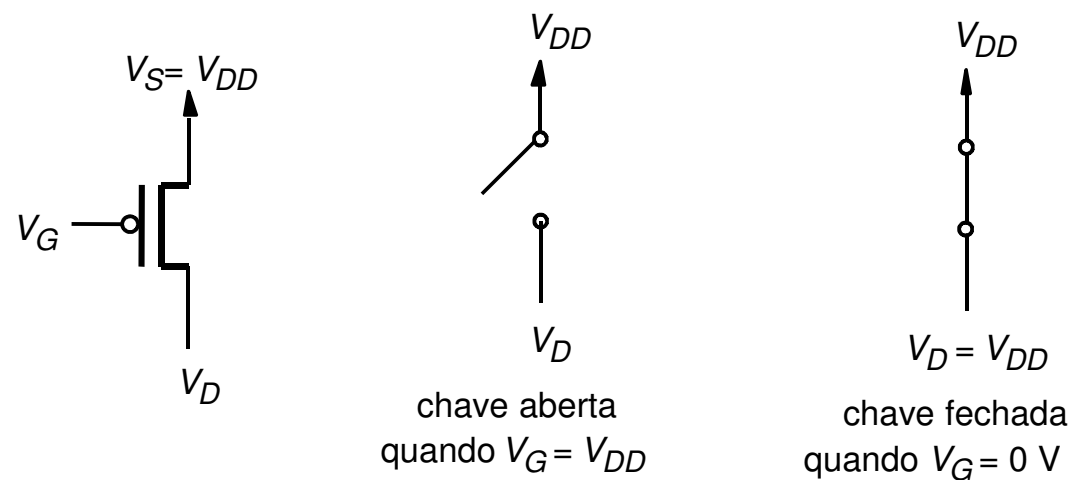
(c) símbolo simplificado para o transistor PMOS

# Transistores NMOS e PMOS em circuitos lógicos

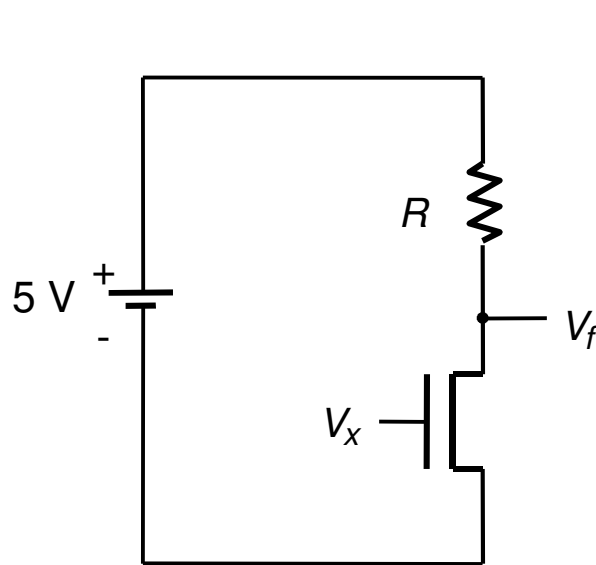
(a) NMOS transistor



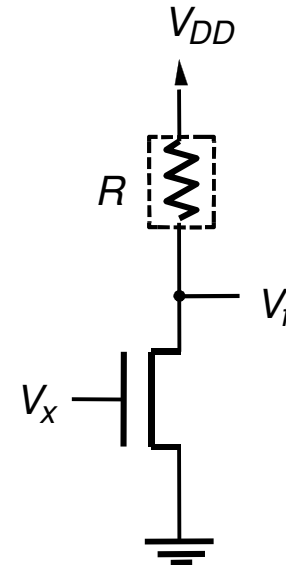
(b) PMOS transistor



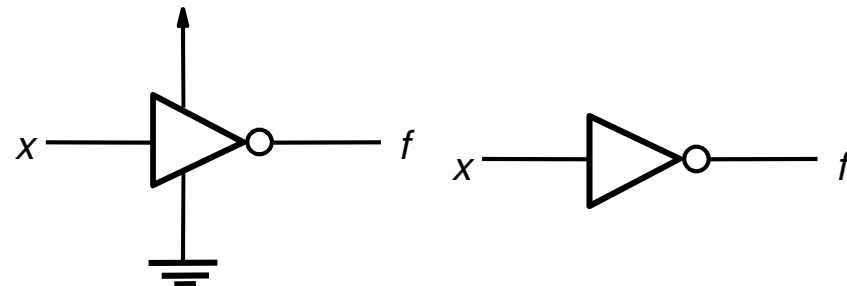
# Porta NOT (inversor) com tecnologia NMOS



(a) Circuito

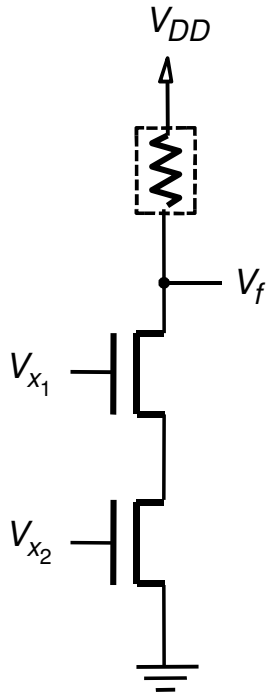


(b) diagrama simplificado do circuito



(c) símbolos gráficos

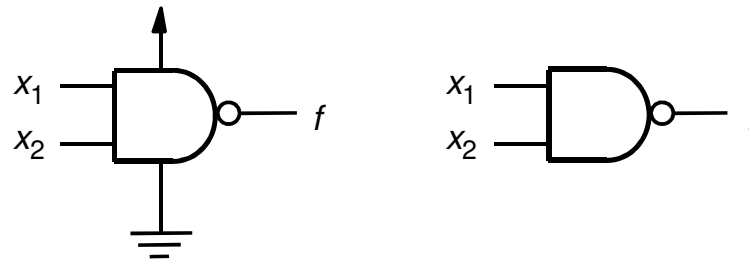
# Porta NAND com tecnologia NMOS



(a) Circuito

$x_1$	$x_2$	$f$
0	0	1
0	1	1
1	0	1
1	1	0

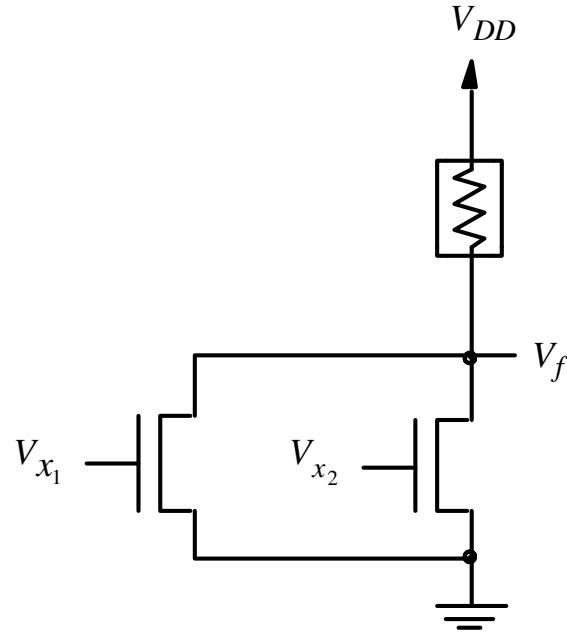
(b) tabela verdade



(c) símbolos gráficos



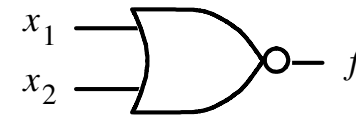
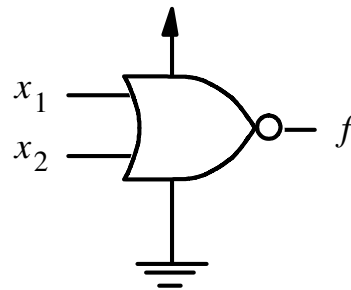
# Porta NOR com tecnologia NMOS



(a) Circuit

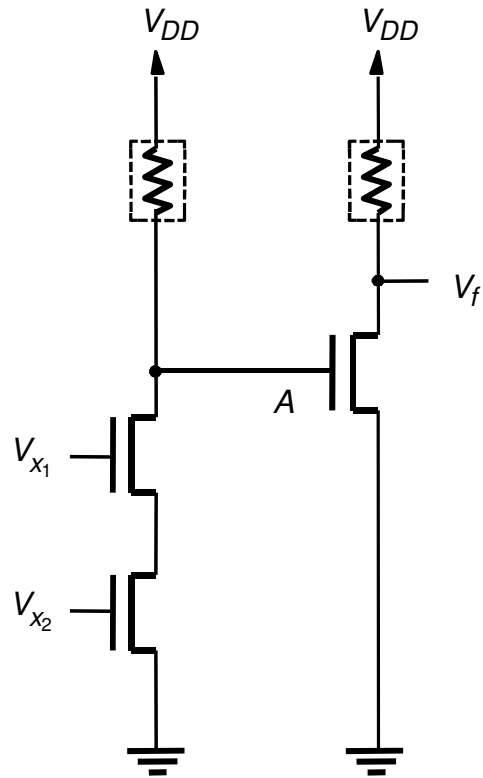
$x_1$	$x_2$	$f$
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table



(c) Graphical symbols

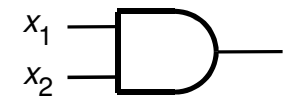
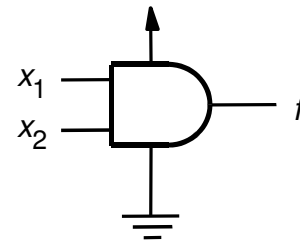
# Porta AND com tecnologia NMOS



(a) Circuito

$x_1$	$x_2$	$f$
0	0	0
0	1	0
1	0	0
1	1	1

(b) tabela verdade

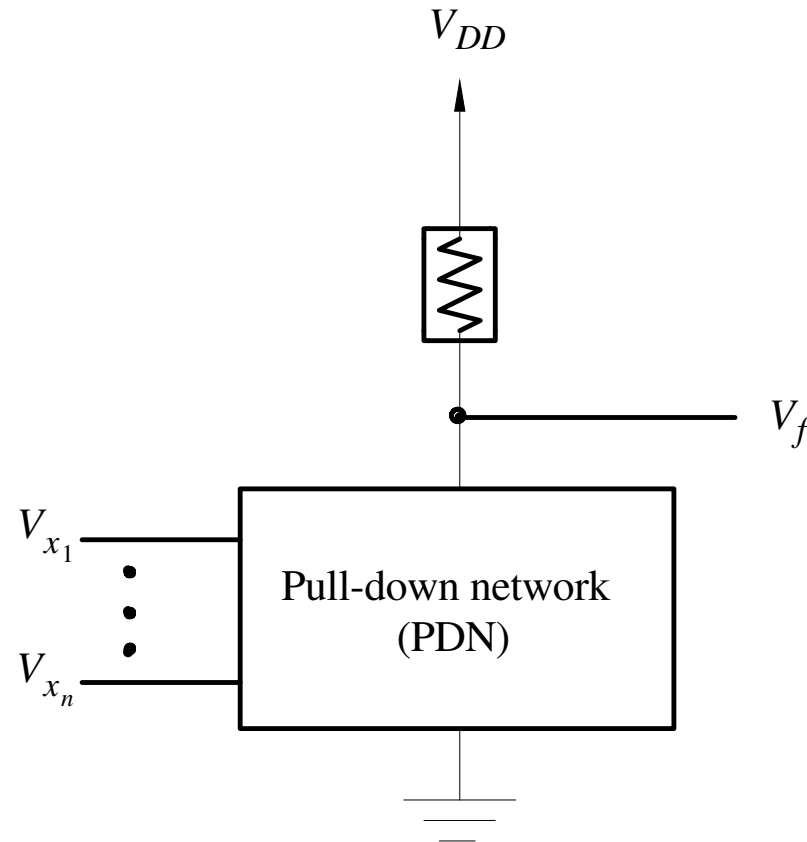


(c) símbolos gráficos

# Estrutura de circuitos NMOS

entradas **definem ou não**  
caminho entre  $V_f$  e terra

se  $V_f = 0$ , então há potência  
estática sendo dissipada  
( $V_{DD} \rightarrow Gnd$ )



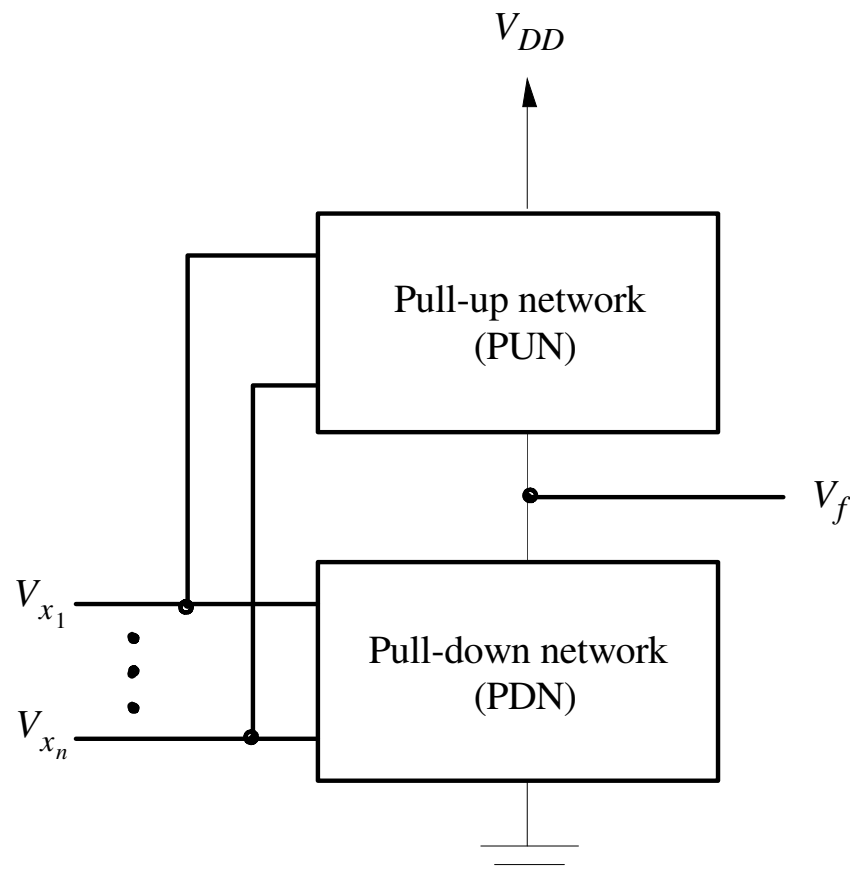
# Estrutura de circuitos CMOS

CMOS: Complementary MOS

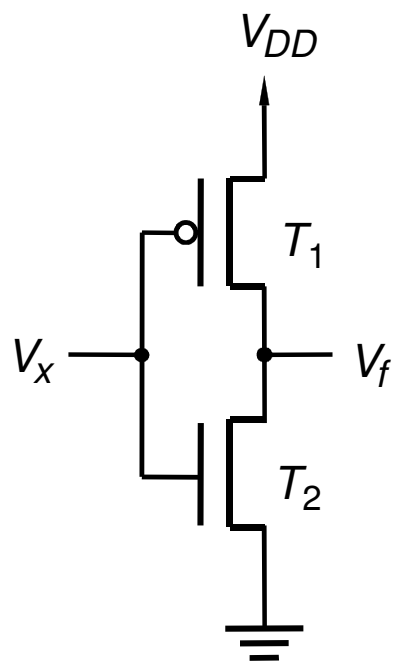
PUN e PDN são redes complementares

Para uma determinada entrada, ou PUN puxa  $V_f$  p  $V_{DD}$  ou PDN baixa  $V_f$  p Gnd

Para qualquer valor de  $V_f$ , não há potência estática sendo dissipada



# Inversor CMOS

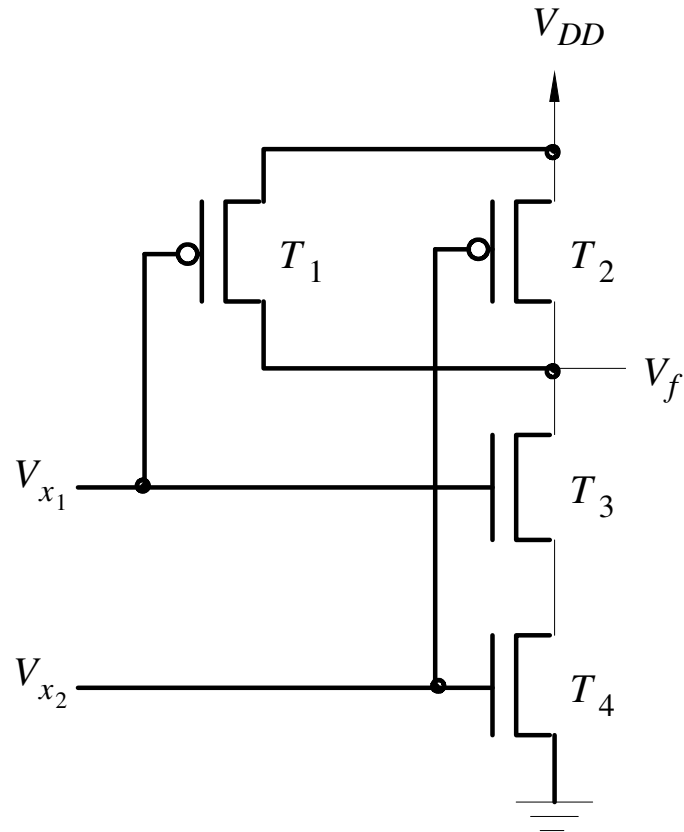


(a) Circuito

$x$	$T_1$	$T_2$	$f$
0	on	off	1
1	off	on	0

(b) Tabela verdade e estado dos transistores

# NAND CMOS

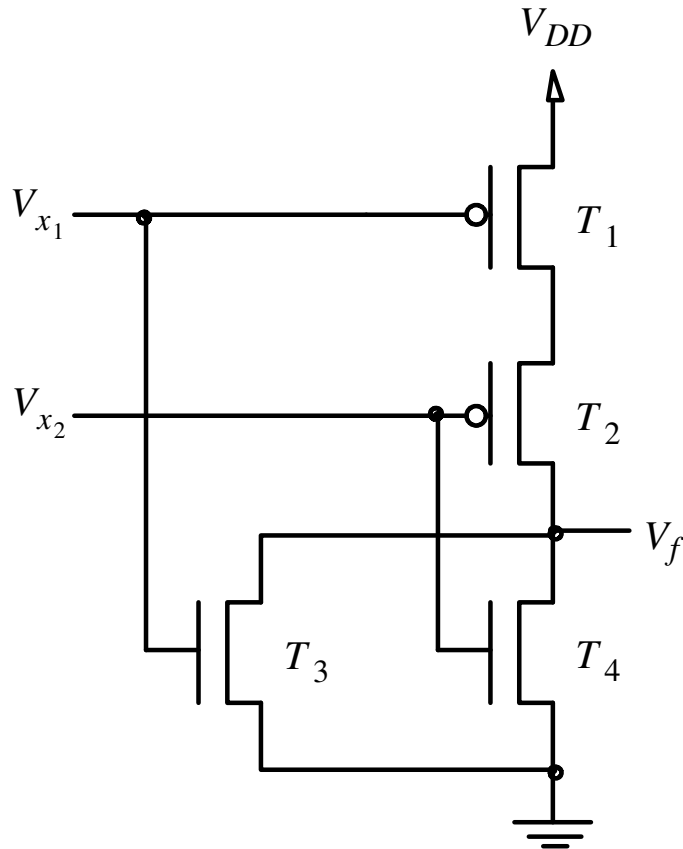


(a) Circuit

$x_1$	$x_2$	$T_1$	$T_2$	$T_3$	$T_4$	$f$
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

# NOR CMOS

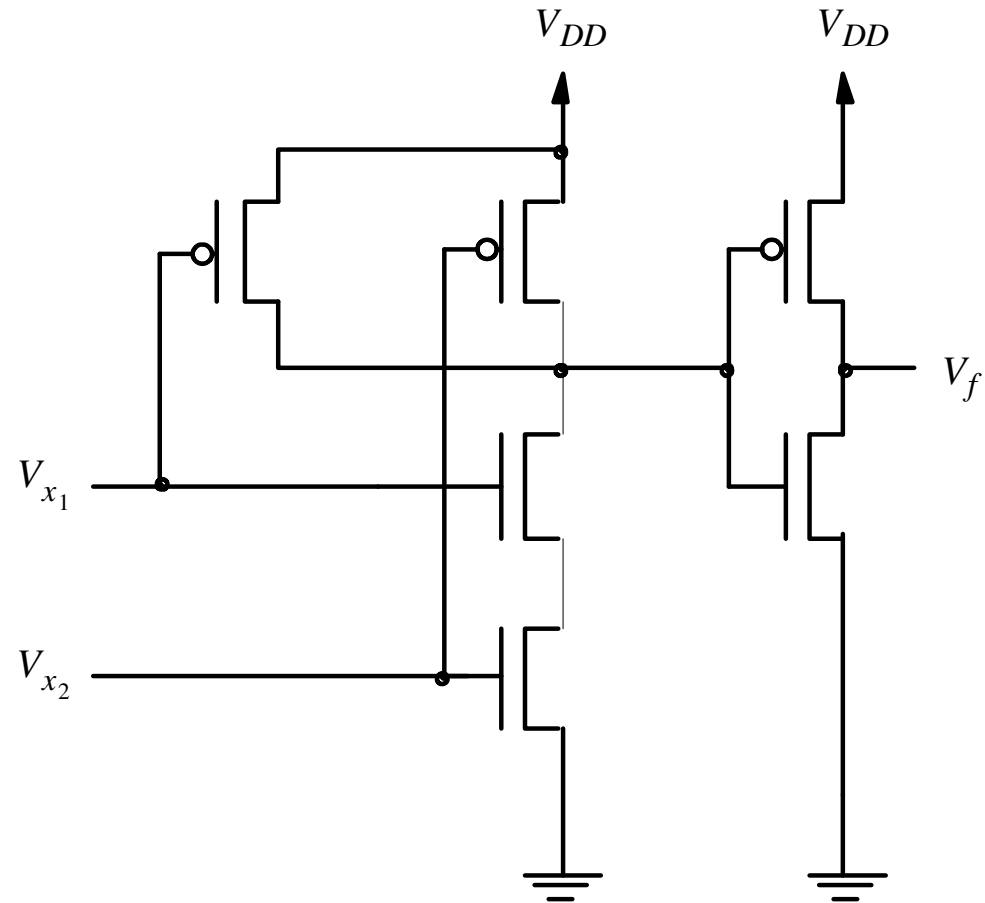


(a) Circuit

$x_1$	$x_2$	$T_1$	$T_2$	$T_3$	$T_4$	$f$
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(b) Truth table and transistor states

# AND CMOS





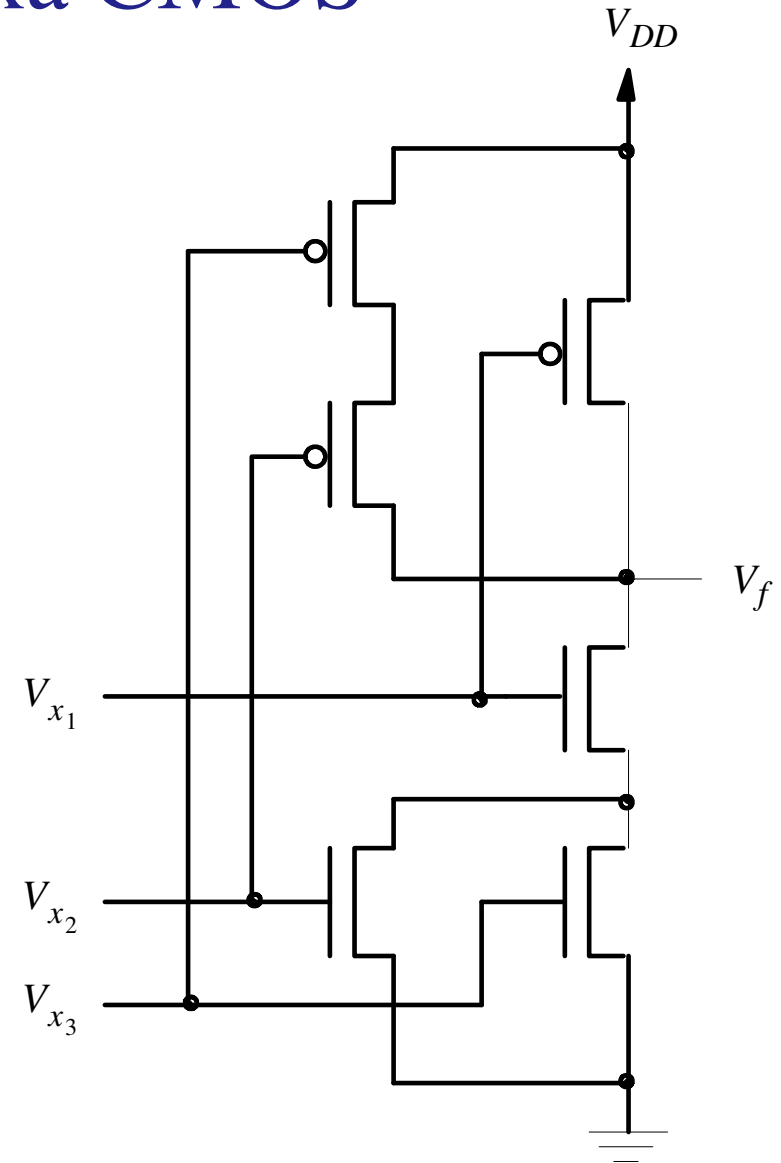
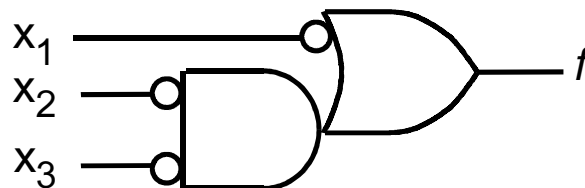
# Uma porta complexa CMOS

$$f = \bar{x}_1 + \bar{x}_2 \cdot \bar{x}_3$$

como variáveis estão  
complementadas  $\rightarrow$  mapeamento  
direto com PUN

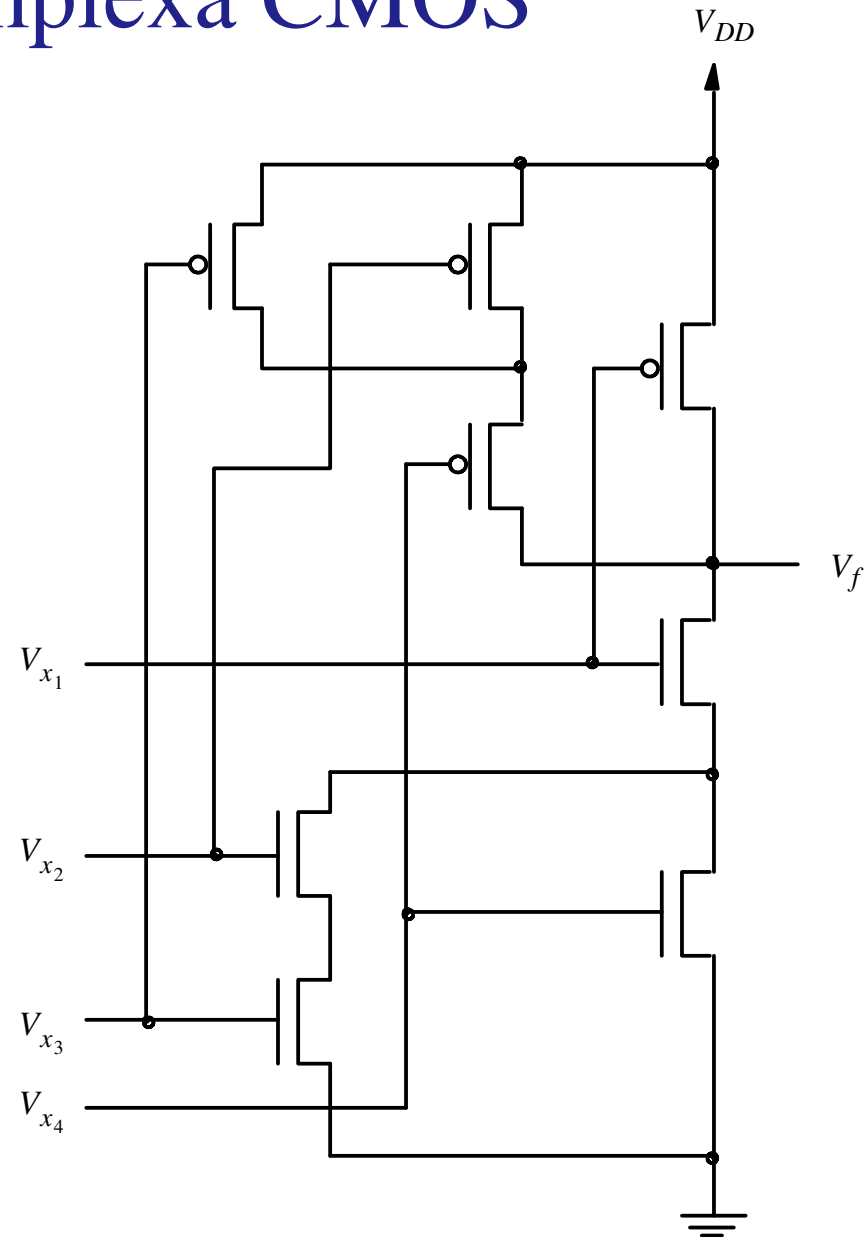
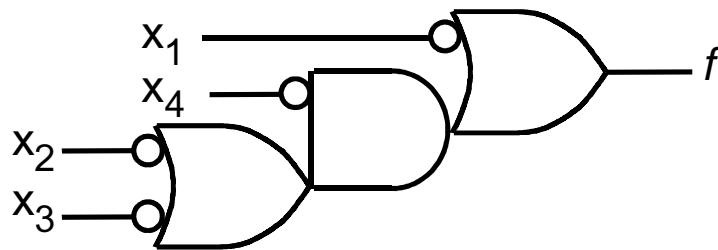
Para o PDN, usar complemento

$$\begin{aligned} \overline{f} &= \overline{\bar{x}_1 + \bar{x}_2 \cdot \bar{x}_3} \\ &= x_1 \cdot (x_2 + x_3) \end{aligned}$$



# Outra porta complexa CMOS

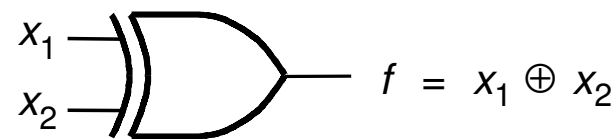
- verificar que PDN é complemento de PUN
- derivar equação da função



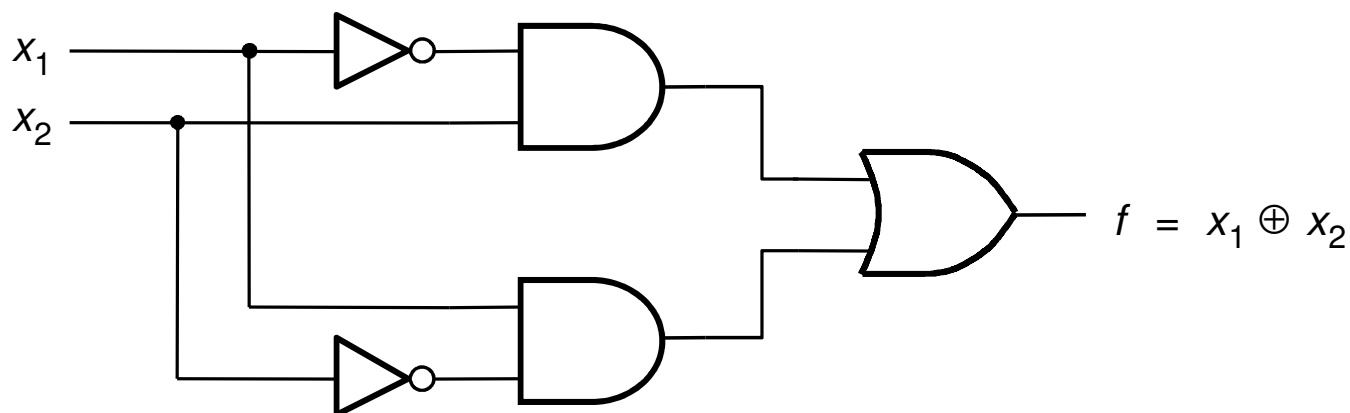
# Porta XOR (Ou exclusivo)

$x_1$	$x_2$	$f = x_1 \oplus x_2$
0	0	0
0	1	1
1	0	1
1	1	0

(a) Tabela verdade



(b) Símbolo

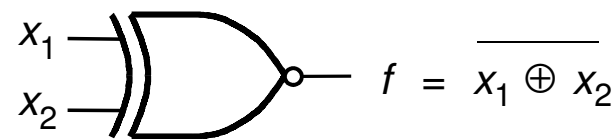


(c) Implementação SOP

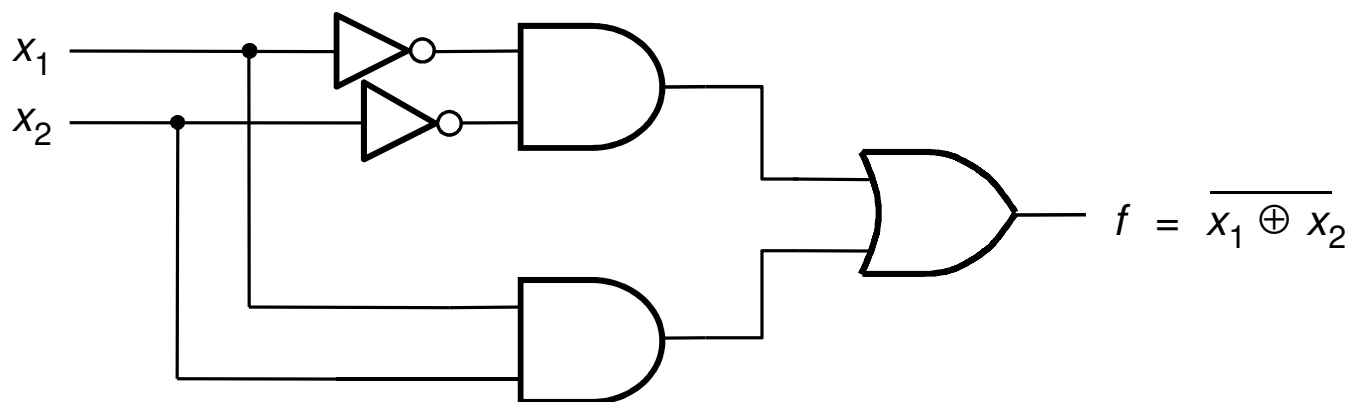
# Porta XNOR

$x_1$	$x_2$	$f = \overline{x_1 \oplus x_2}$
0	0	1
0	1	0
1	0	0
1	1	1

(a) Tabela verdade



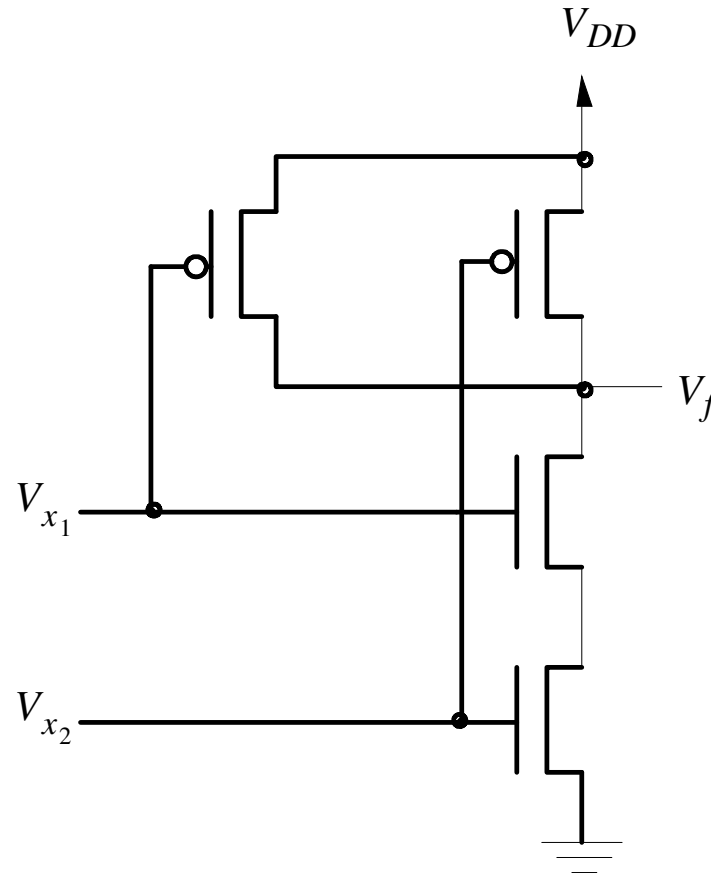
(b) Símbolo



(c) Implementação SOP

# Lógica positiva ou negativa

- L=low
- H=high
- lógica positiva  
L → "0"  
H → "1"
- lógica negativa  
L → "1"  
H → "0"



(a) Circuit

$V_{x_1}$	$V_{x_2}$	$V_f$
L	L	H
L	H	H
H	L	H
H	H	L

(b) Voltage levels

- Usaremos  
Lógica Positiva

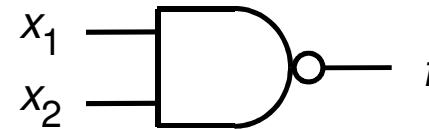
# Duas interpretações para um mesmo circuito

$V_{x_1}$	$V_{x_2}$	$V_f$
L	L	H
L	H	H
H	L	H
H	H	L

(a) Níveis de voltagem

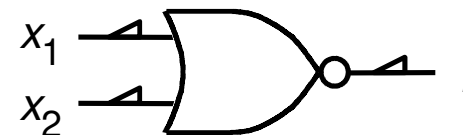
$x_1$	$x_2$	$f$
0	0	1
0	1	1
1	0	1
1	1	0

(b) Tabela verdade com lógica positiva e símbolo lógico



$x_1$	$x_2$	$f$
1	1	0
1	0	0
0	1	0
0	0	1

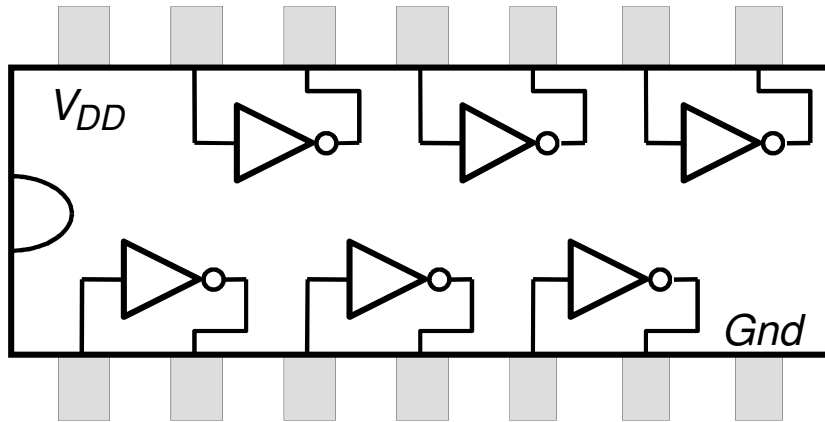
(c) Tabela verdade com lógica negativa e símbolo lógico



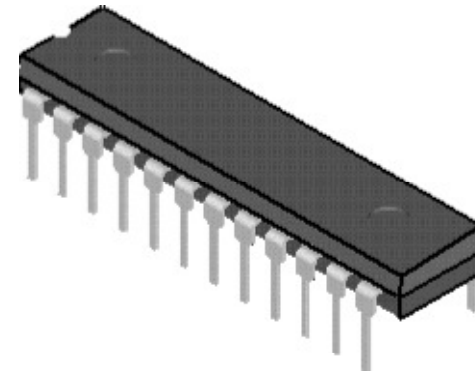
# Tipos de tecnologia de implementação

- SSI, MSI, LSI, VLSI =
  - (small | medium | large | very-large) scale integration
- Circuitos comerciais (SSI e MSI): série 7400
- Circuitos programáveis (em bancada)
  - PLAs (Programmable Logic Array), PLD (... Device), CPLD (Complex .....
  - FPGA: Field Programmable Gate Array
- Circuitos integrados:
  - Gate Array: gates prefabricados e interligados no último passo da fabricação
  - Std Cell: células mais complexas, interligadas no último passo da fabricação
  - Full Custom: totalmente customizados

# A série 7400 de chips comerciais



(b) Estrutura de um chip 7404

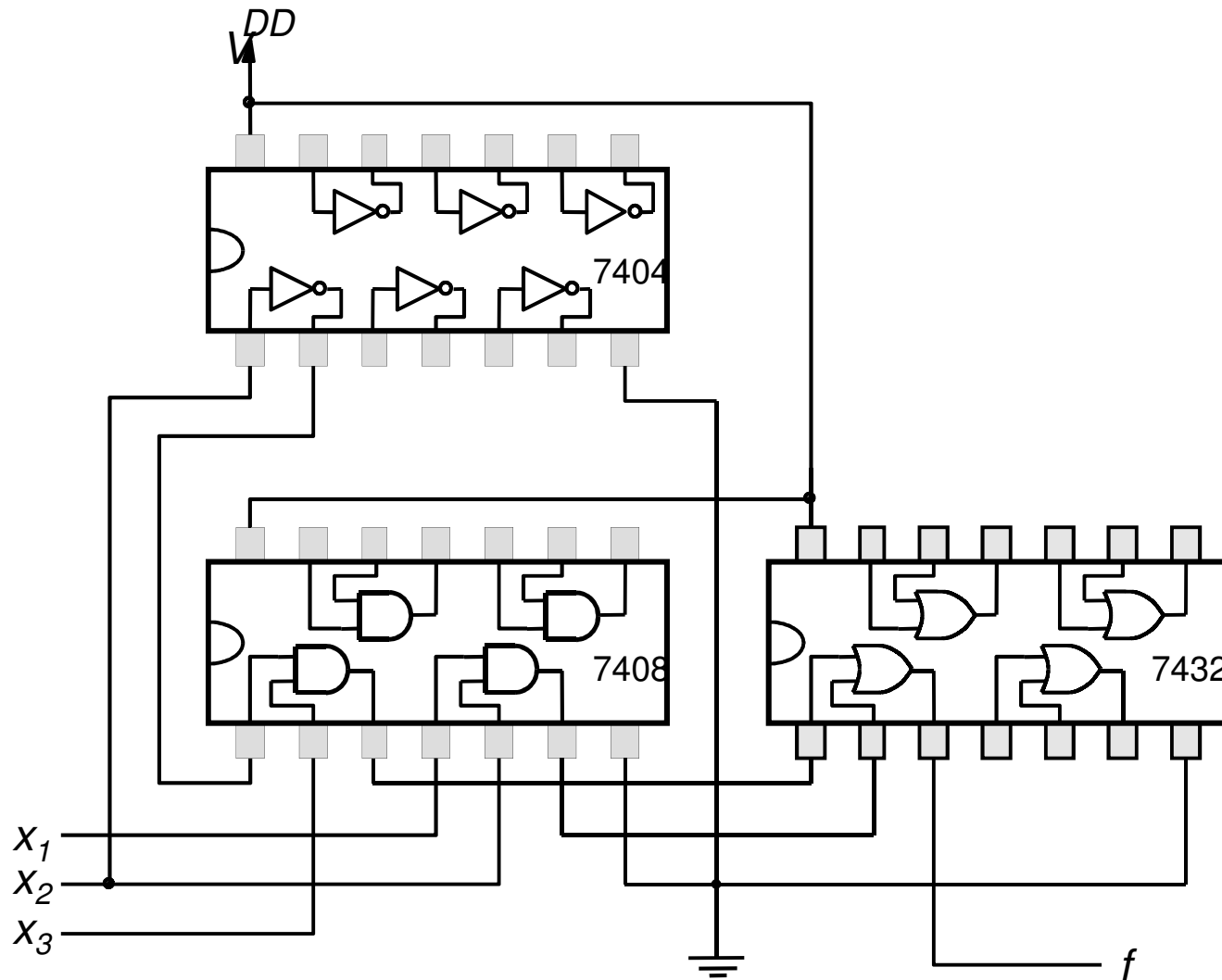


(a) Dual-inline package (DIP)

- Procurar na web datasheets de componentes comerciais da família 7400

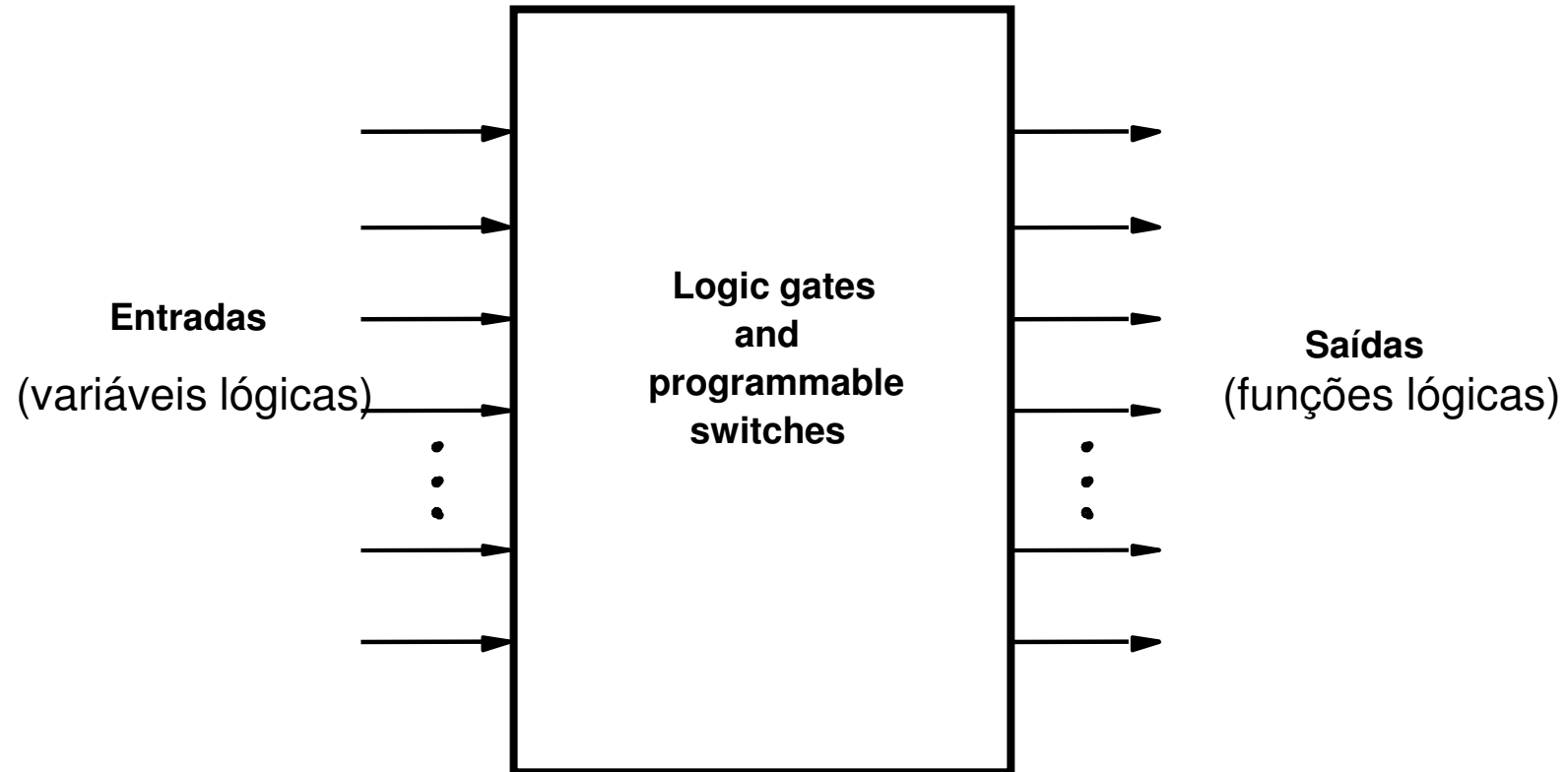


# Implementação de uma função



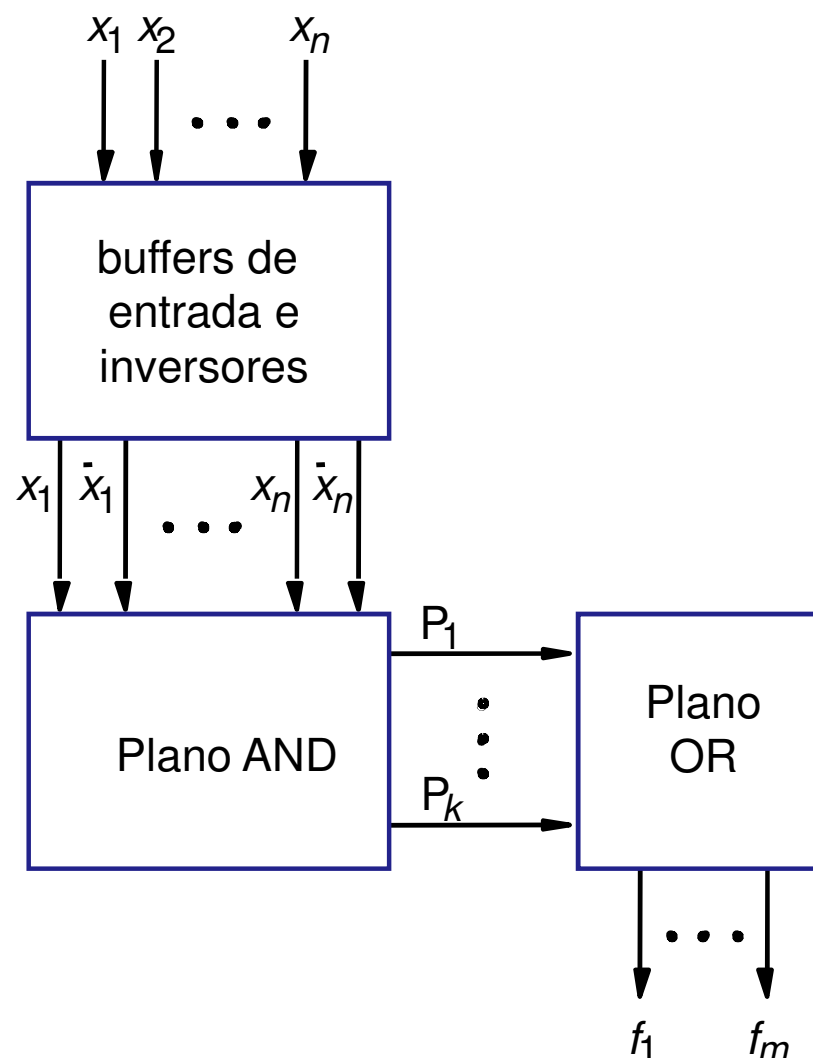
Implementação de  $f = x_1 \cdot x_2 + \overline{x_2} \cdot x_3$

# Dispositivo programável como caixa preta

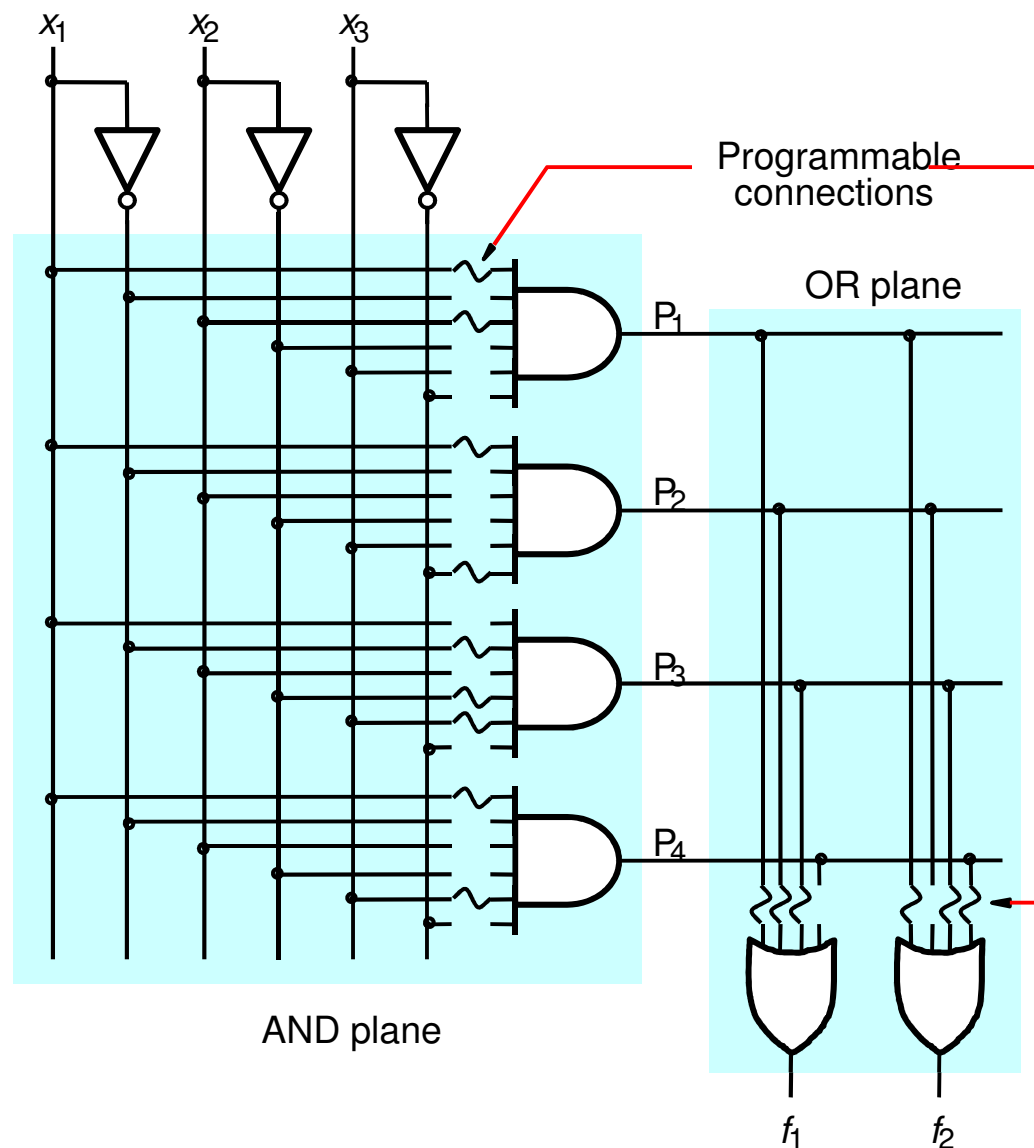


# Estrutura de uma PLA

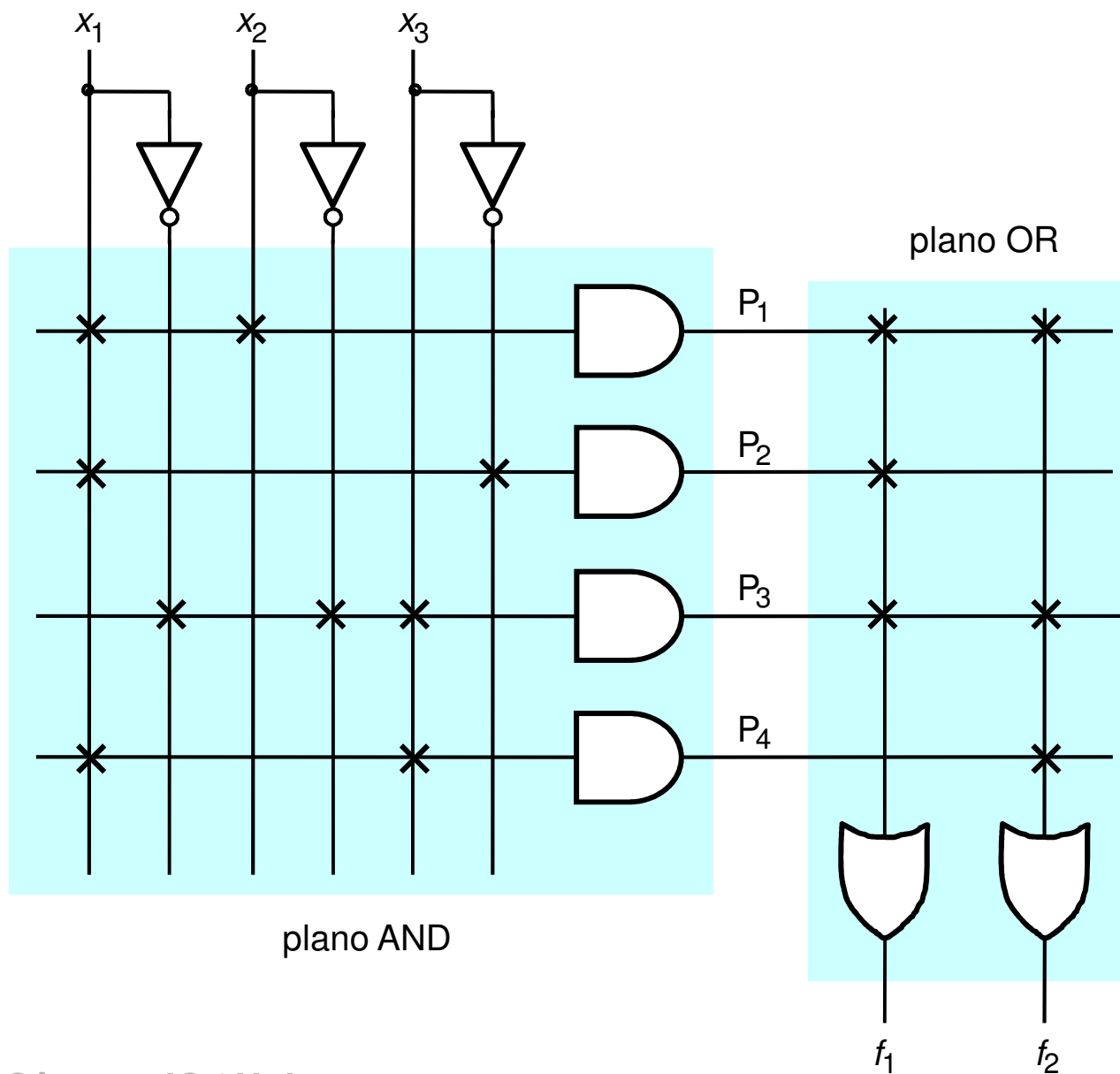
- Baseada em SOP
- Todas entradas disponíveis (verdadeiro e complementado)
- Saídas do plano AND: Produtos  $P_1$  a  $P_k$
- Saídas do plano OR: somas de Produtos = funções das saídas  $f_1$  a  $f_m$



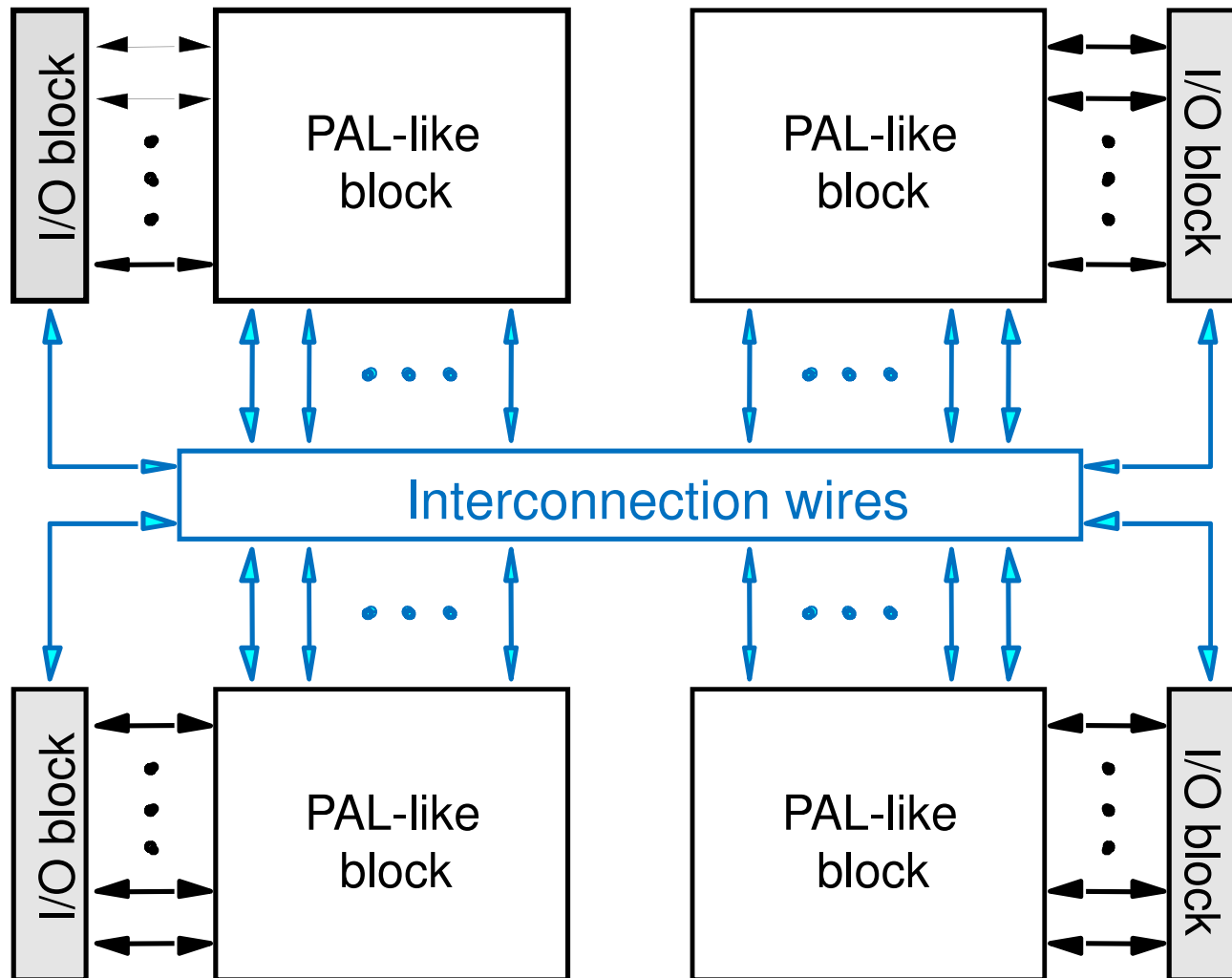
# PLA: visão no nível de gate



# PLA: visão simplificada



# Estrutura de uma CPLD típica





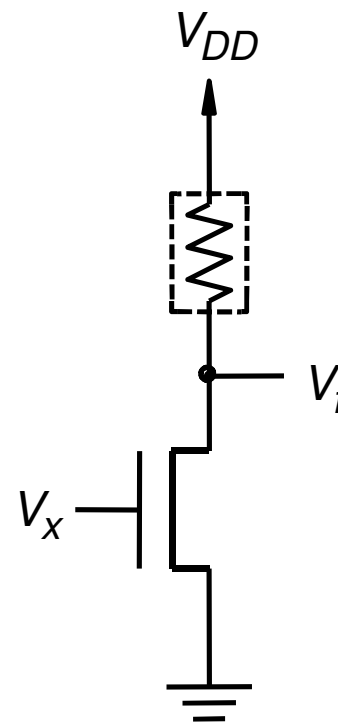
# Características elétricas

- Níveis
- Margem de ruído
- Potência dissipada
  - estática
  - dinâmica

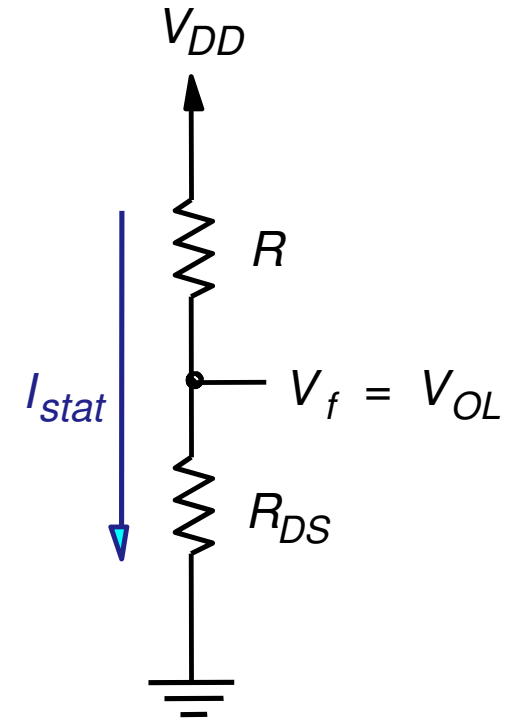
# Níveis elétricos em um inversor NMOS

- se  $V_x = 0 \rightarrow V_f = V_{DD}$
- se  $V_x = 5V \rightarrow V_f = V_{OL}$   
definido pelo div. de tensão

$$V_{OL} = V_{DD} \cdot \frac{R_{DS}}{R_{DS} + R}$$



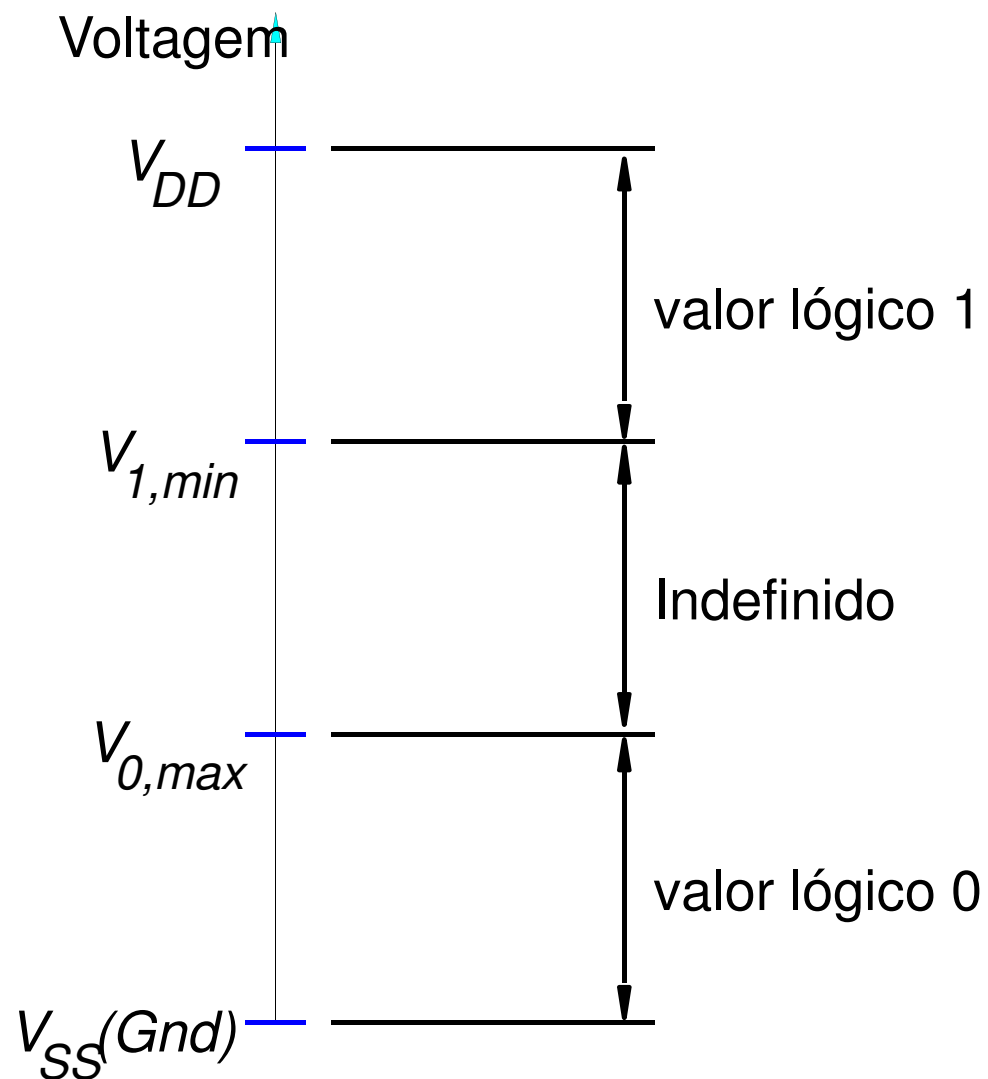
(a) inversor NMOS



(b)  $V_x = 5V$

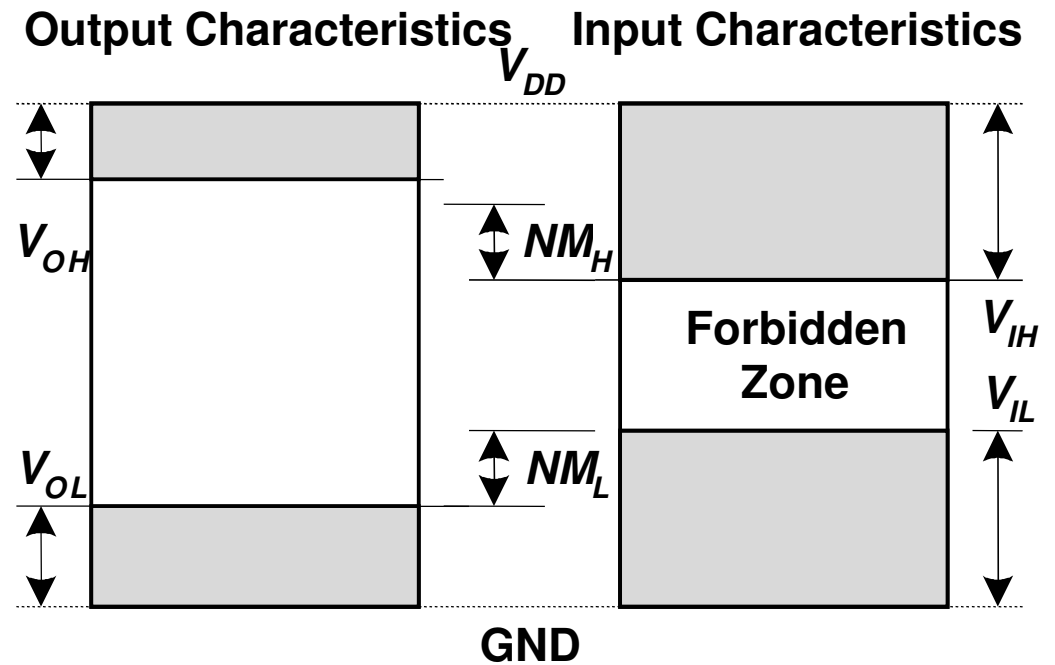
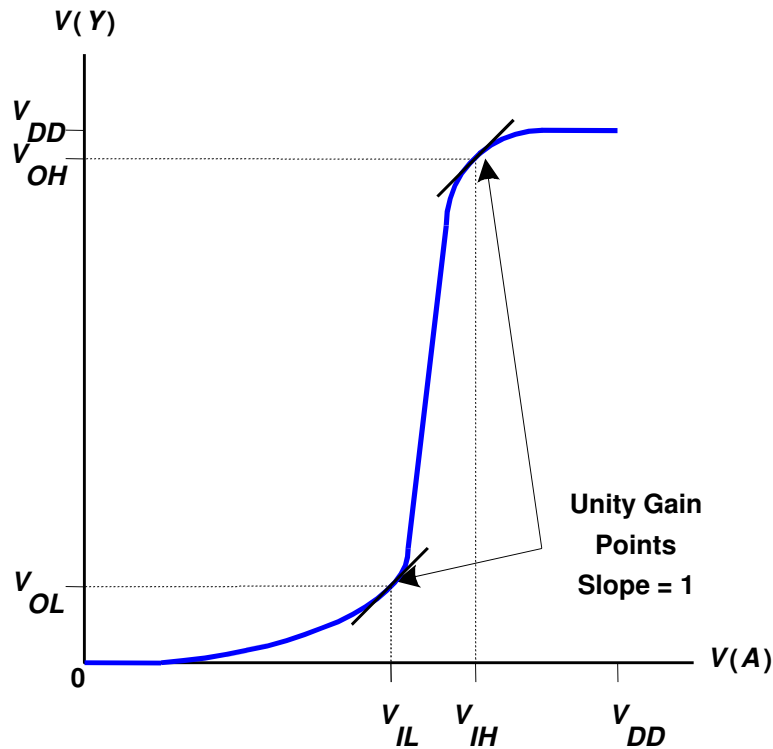
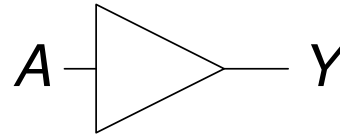


# Níveis Lógicos

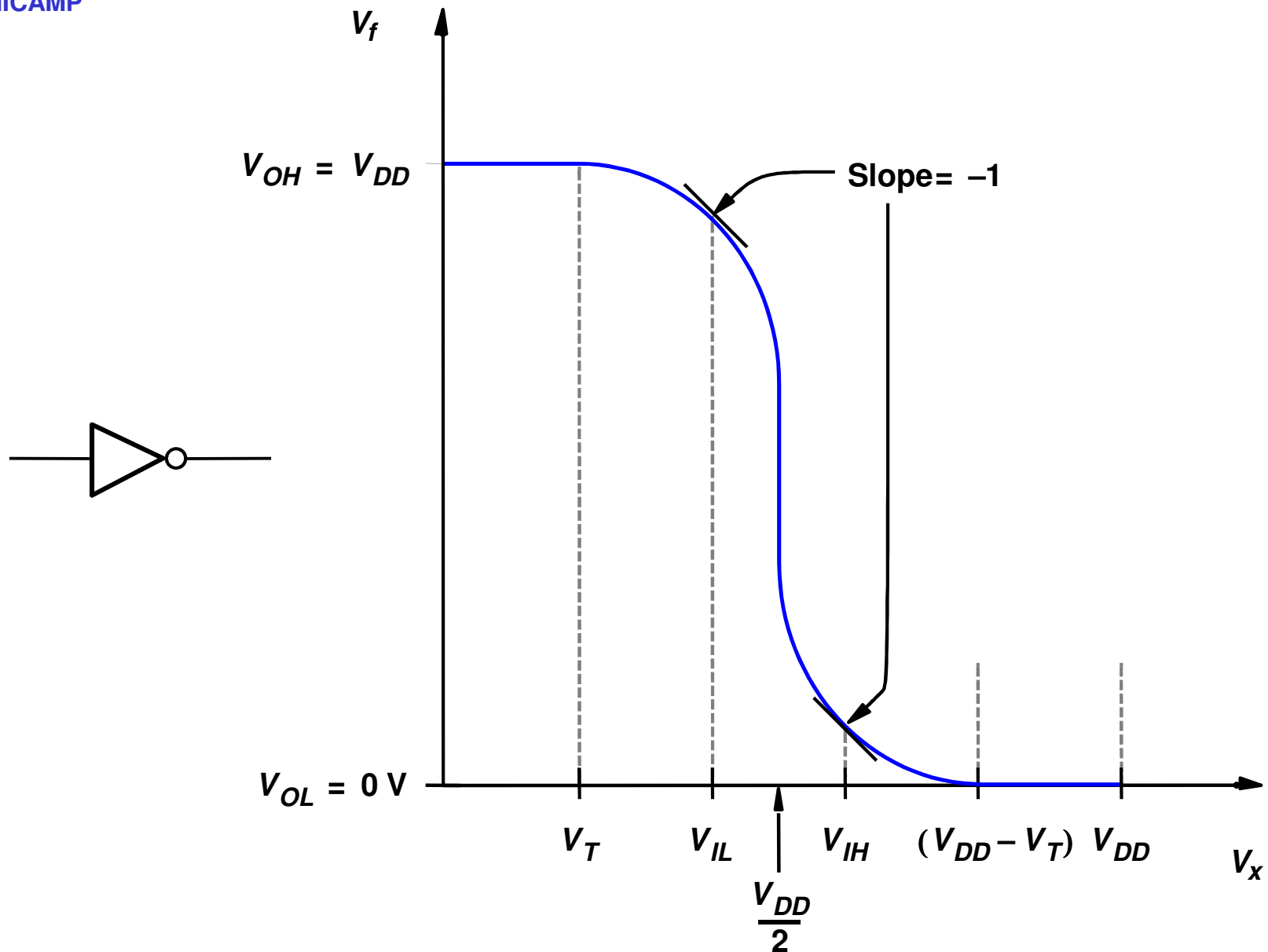




# Característica de Transferência DC



# Característica de Transferência DC



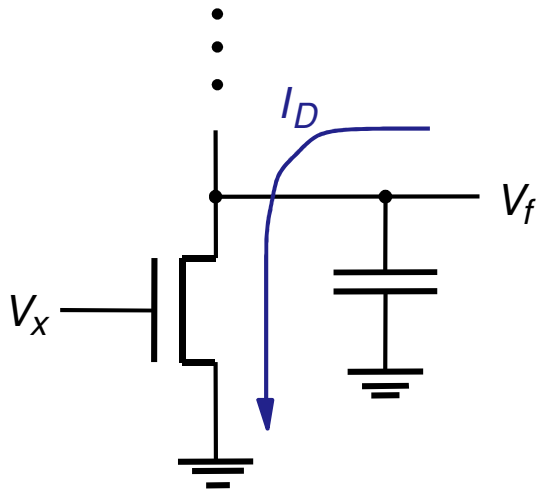
# Margem de ruído para algumas tecnologias

- Outra vantagem do CMOS

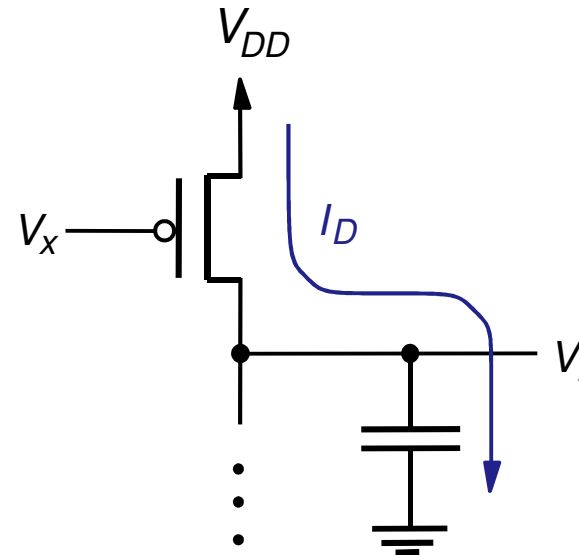
**Noise Margin**

--	<b>VOH</b>	<b>VIH</b>	<b>Margin</b>	<b>VIL</b>	<b>VOL</b>	<b>Margin</b>
TTL [5volt]	2.4v	2.0v	400mV	0.8v	0.5v	300mV
FCT [5volt]	2.5v	2.0v	500mV	0.8v	0.5v	300mV
BTL [5 volt]	2.1v	1.62v	480mV	1.47v	1.1v	370mV
GTL [5 volt]	1.5v	1.05v	450mV	0.95v	0.55v	400mV
CMOS [5 volt]	4.9v	3.85v	1050mV	1.35v	0.1	1340mV
LVTTL [3volt]	2.4v	2.0v	400mV	0.8v	0.4v	400mV
LVC MOS [3 volt]	2.8v	2.0v	800mV	0.8v	0.2v	600mV
CMOS [2.5v]	2.0v	1.7v	300mV	0.7v	0.4v	300mV
CMOS [1.8v]	1.35v	1.1v	250mV	0.66v	0.45v	210mV

# Potência dinâmica em CMOS



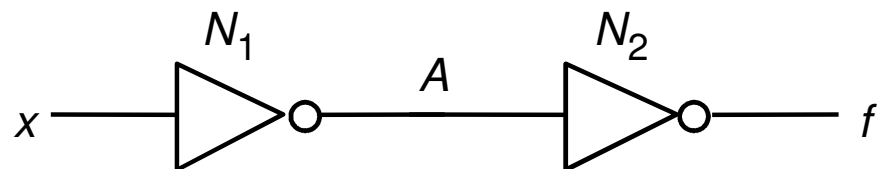
(a) Fluxo de corrente quando  $V_x$  muda de 0 V para 5 V



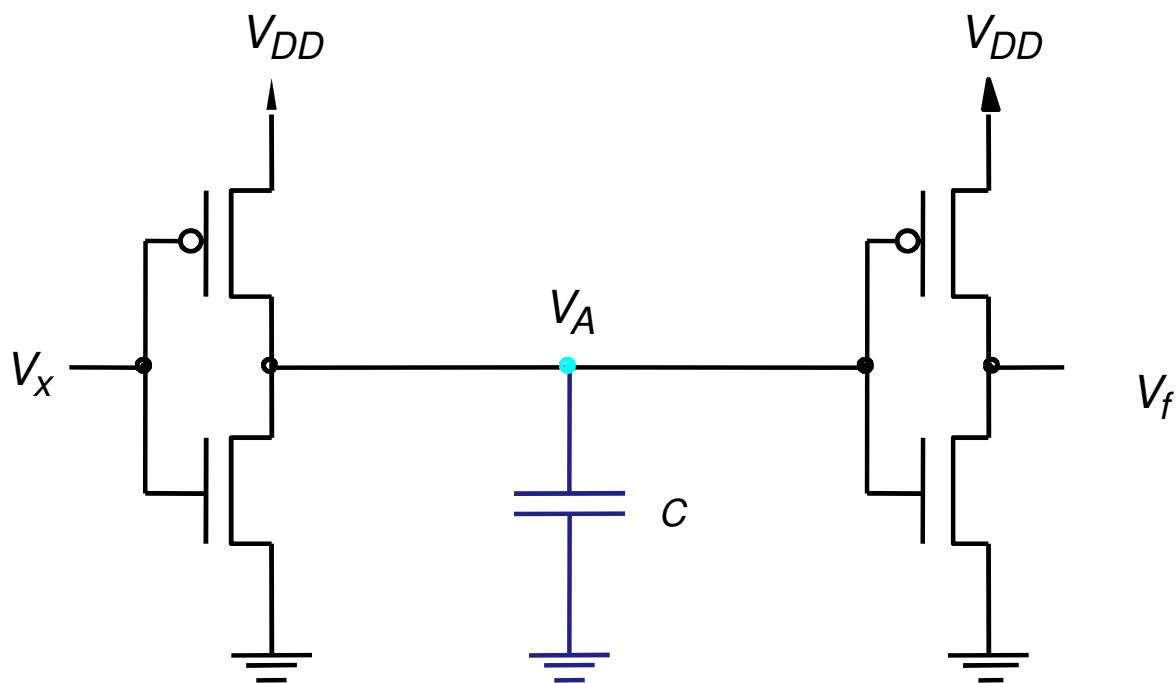
(a) Fluxo de corrente quando  $V_x$  muda de 5 V para 0 V

- Pot. dinâmica dissipada proporcional à  $C \cdot V_{dd}^2 \cdot f$
- $C$  = soma das capacitâncias do circuito

# Atraso: capacitância parasita

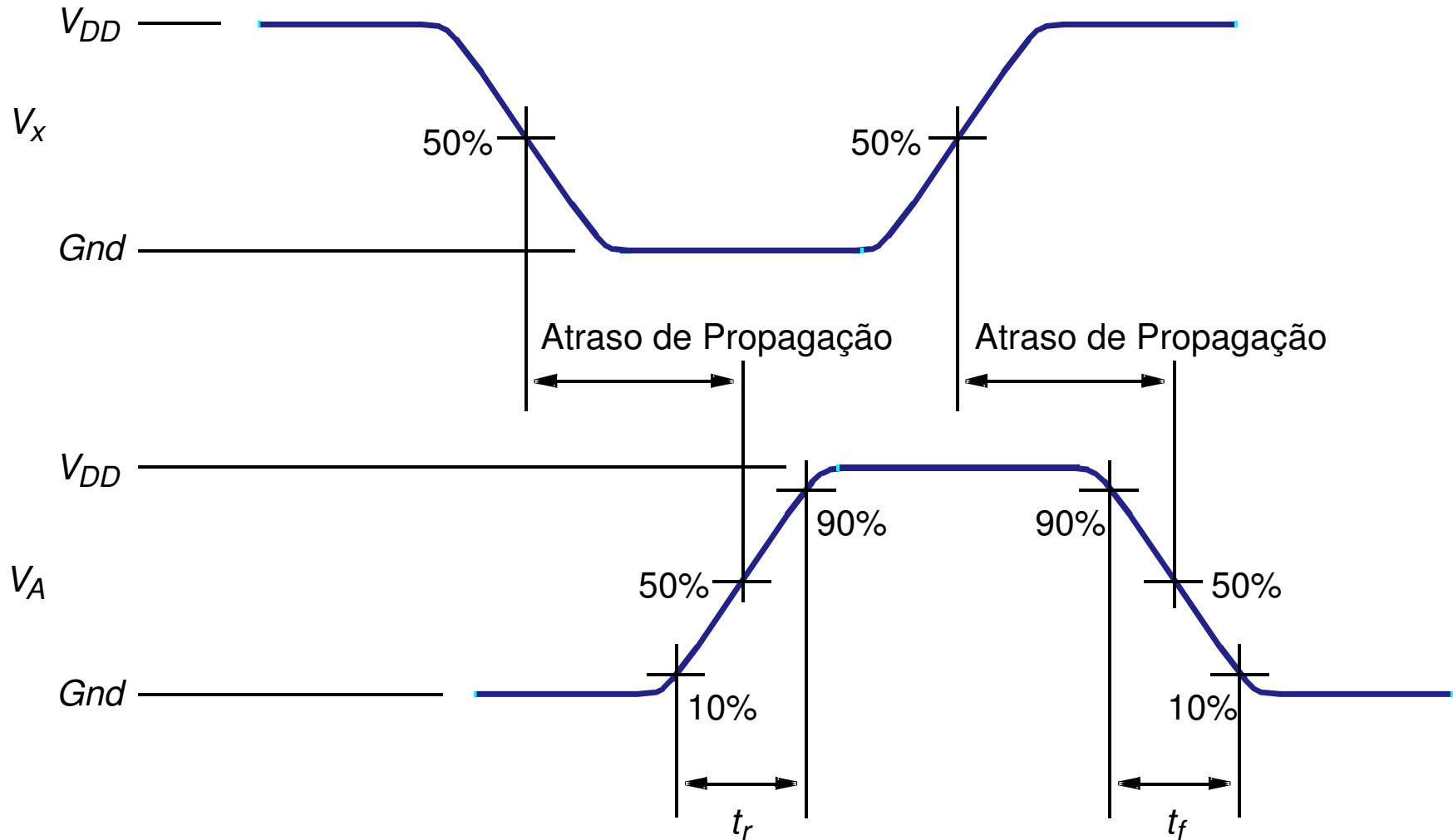


(a) Um inversor acionando outro inversor



(b) Carga capacitiva no nó A

# Forma de onda: tempos importantes



$t_r$ : tempo de subida (rising)

$t_f$ : tempo de descida (falling)

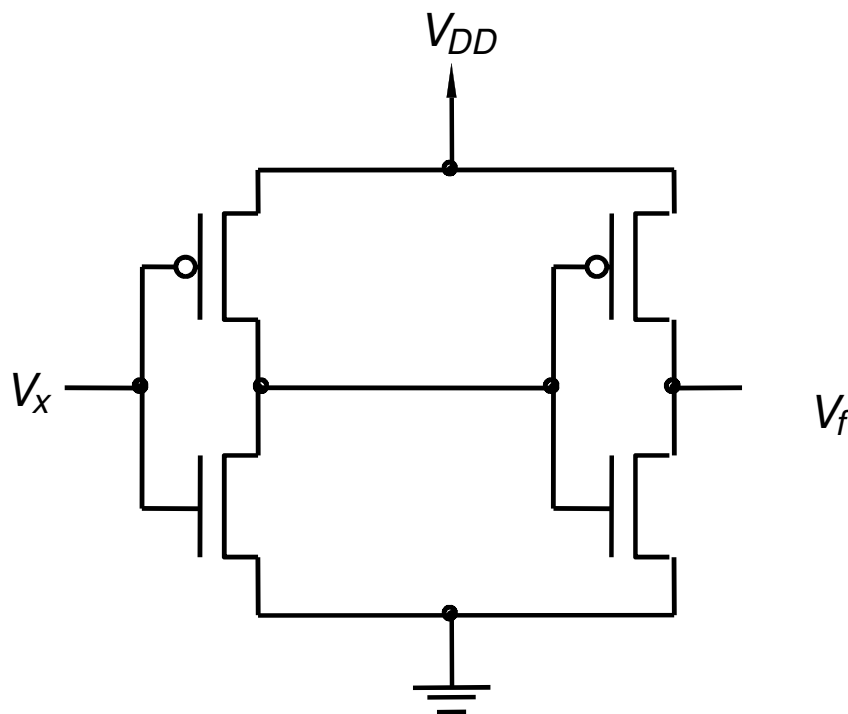




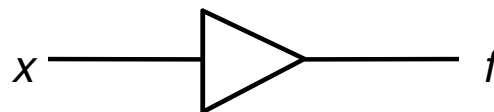
## Fan-in e fan-out em uma porta lógica

- Fan-in:  $n^{\circ}$  de entradas de uma porta lógica
  - se for muito grande  $\rightarrow$  resistência grande (transistores em série)  $\rightarrow$  atraso de propagação grande
- Fan-out:  $n^{\circ}$  de portas acionadas por uma saída
  - se for muito grande  $\rightarrow$  capacitância grande (várias entradas sendo acionadas)  $\rightarrow$  atraso de propagação grande
- Fan-in e fan-out devem ser limitadas para não afetar o desempenho do circuito

# Buffer não inversor

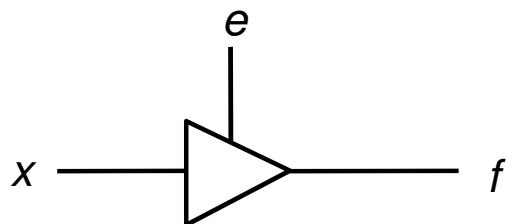


(a) implementação

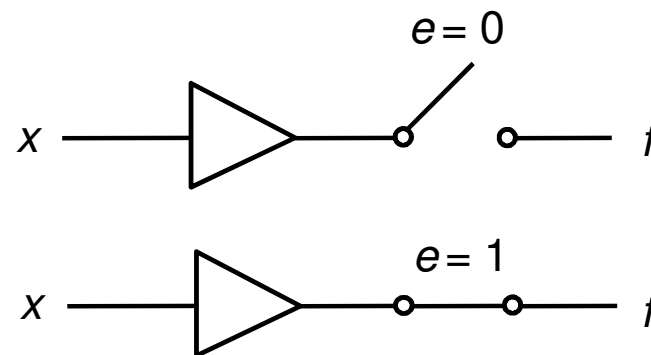


(b) símbolo

# Buffer tri-state



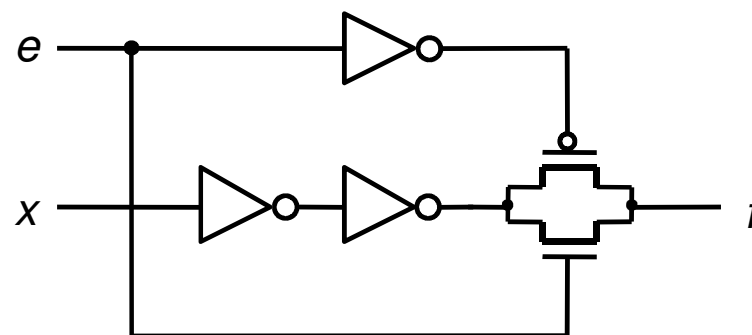
(a) Buffer tri-state



(b) Circuito equivalente

<i>e</i>	<i>x</i>	<i>f</i>
0	0	Z
0	1	Z
1	0	0
1	1	1

(c) Tabela verdade



(d) Implementação

# Circuitos comerciais série 7400

- Bipolar
  - 74 - "standard TTL"
  - 74L - Low power
  - H - High speed
  - S - Schottky
  - LS - Low Power Schottky
  - AS - Advanced Schottky
  - ALS - Advanced Low Power Schottky
  - F - Fast (faster than normal Schottky, similar to AS)
- CMOS
  - C - CMOS 4–15 V (semelhante a 4000 series)
  - HC - High speed CMOS,
  - HCT - High speed, níveis compatíveis com bipolar

# Datasheet típica

- Procurar na web
- Amostras no site do curso (material complementar)
  - 74HC51: 2 AOI (AND-OR-INVERT)
  - 74HC153: 2 MUX 4:1
- Identificar especificações
  - lógica funcional
  - características elétricas:  $V_{IH}$ ,  $V_{IL}$ ,  $V_{OH}$ ,  $V_{OL}$
  - características dinâmicas:  $tp_{LH}$ ,  $tp_{HL}$