Problem	Separation Strategy	LP value	% GAP	UB	OPT		B & C Nodes	CPU time (m)	
vlsi.166.4.504	C,P,K,S,E	133.9412	51.29	275	-		1	131:56	
vlsi.37.4.92	C,P,K,S,E	118.0287	0.82	119	119	*	1	3:51	
vlsi.38.4.105	C,P,K,S,E	234.0598	2.07	239	-		2	60:23	(59:03)
vlsi.43.4.105	C,P,K,S,E	118.5000	1.25	120	120	*	5	15:13	(12:21)
vlsi.48.4.81	C,P,K,S,E	44.7492	35.15	69	-		10	60:07	(12:30)
vlsi.17.4.39	C,P,K,S,E	41.1840	6.40	44	44	*	15	22:03	(4:28)