exception handling. It has a number of system exceptions plus a number of external Interrupt Request (IRQs) (external interrupt inputs). There is no fast interrupt (FIQ) (fast interrupt in ARM7/ARM9/ARM10/ARM11) in the Cortex-M3; however, interrupt priority handling and nested interrupt support are now included in the interrupt architecture. Therefore, it is easy to set up a system that supports nested interrupts (a higher-priority interrupt can override or preempt a lower-priority interrupt handler) and that behaves just like the FIQ in traditional ARM processors.

The interrupt features in the Cortex-M3 are implemented in the NVIC. Aside from supporting external interrupts, the Cortex-M3 also supports a number of internal exception sources, such as system fault handling. As a result, the Cortex-M3 has a number of predefined exception types, as shown in Table 2.2.

### 2.9.1 Low Power and High Energy Efficiency

The Cortex-M3 processor is designed with various features to allow designers to develop low power and high energy efficient products. First, it has sleep mode and deep sleep mode supports, which can work with various system-design methodologies to reduce power consumption during idle period.

**Table 2.2** Cortex-M3 Exception Types

| Exception Number | Exception Type | Priority (Default to 0 if Programmable) | Description |
| --- | --- | --- | --- |
| 0 | NA | NA | No exception running |
| 1 | Reset | −3 (Highest) | Reset |
| 2 | NMI | −2 | NMI (external NMI input) |
| 3 | Hard fault | −1 | All fault conditions, if the corresponding fault handler is not enabled |
| 4 | MemManage fault | Programmable | Memory management fault; MPU violation or access to illegal locations |
| 5 | Bus fault | Programmable | Bus error (prefetch abort or data abort) |
| 6 | Usage fault | Programmable | Program error |
| 7–10 | Reserved | NA | Reserved |
| 11 | SVCall | Programmable | Supervisor call |
| 12 | Debug monitor | Programmable | Debug monitor (break points, watchpoints, or external debug request) |
| 13 | Reserved | NA | Reserved |
| 14 | PendSV | Programmable | Pendable request for system service |
| 15 | SYSTICK | Programmable | System tick timer |
| 16 | IRQ #0 | Programmable | External interrupt #0 |
| 17 | IRQ #1 | Programmable | External interrupt #1 |
| … | … | … | … |
| 255 | IRQ #239 | Programmable | External interrupt #239 |

*The number of external interrupt inputs is defined by chip manufacturers. A maximum of 240 external interrupt inputs can be supported. In addition, the Cortex-M3 also has an NMI interrupt input. When it is asserted, the NMI-ISR is executed unconditionally.*